From: lisa
Sent: Thursday, December 01, 1994 10:22 AM
To: 'djc'
Subject: Re: odd terp message

```
> From hayes@MicroUnity.com Wed Nov 30 21:17:54 1994
> Return-Path: <hayes@MicroUnity.com>
> Received: from erato.microunity.com by gaea.microunity.com (4.1/muse1.3)
>     id AA02967; Wed, 30 Nov 94 21:17:52 PST
> Received: by erato.microunity.com (931110.SGI/930416.SGI)
>     for jerry@sisyphus.microunity.com id AA12514; Wed, 30 Nov 94
21:17:50 -0800
> Date: Wed, 30 Nov 94 21:17:50 -0800
> From: hayes@MicroUnity.com (Raymond R. Hayes)
> Message-Id: <9412010517.AA12514@erato.microunity.com>
> To: lisa@MicroUnity.com, jerry@MicroUnity.com
> Subject: Pentium humor
>
>
>
> >Did you hear about the new "morning after" pill being developed as a
replacement
> >for RU-486???
>
> >Its called RU-Pentium.  It causes the embryo to not divide correctly.
>
>
>
```

Sorry if you just got a null reply from me -- mail just did something really weird!

> At the time I wrote this test, the cache sizing in terp did not look
> at the cerb octlet 6 value.

Yeah, that's true, but why were you writing 16k into the sizes anyway?
That's guaranteed to cause your test to bomb on the hardware!

> It sounds like it now does the sizing dynamically based on the cerb
> octlet. Is that correct?

Yep, as long as you don't provide any command-line overrides.
Setting the cache or buffer size on the command line means I have to make a guess about
the configuration you really want, since you could be asking for more than the hardware
actually provides.
(Which, by the way, you were, when setting the cache size to 16k and still expecting 32k
of buffer.) This usually just results in the simulator allocating more stuff than
necessary.

lisa

From:	lisar (Lisa Robinson)
Sent:	Thursday, December 01, 1994 11:00 AM
To:	'doi (Derek Iverson)'
Cc:	'doi'; 'gmo'; 'gregg'; 'guarino'; 'hestia'; 'iimura'; 'jeffm'; 'sandeep'; 'wayne'
Subject:	Software Bring-up Meeting - November 30, 1994

Derek Iverson wrote (on Wed Nov 30):

    Item: Get the cycle count for oc-mem test that ran on the hardware
            simulator.
    Who: doi
    Status: [11/30] new.

            Derek will ask lisar if the data is still around.

No, the data is too large to keep lying around. I am running oc-barrel now though. I think
alot can be gained by looking at much smaller code segments than these.

    Item: What is dependent on SC within Euterpe? ROM & LEDs?
            Reads of cerberus registers?
    Who: wayne
    Status: [11/23] No progress.

Fire this question at dickson

    We also decided to start tracking the progress of running tests on
    the hardware simulator in this meeting.

How about tracking the status of running the tests on the software simulator too and not
just whether they run, what features need to be added to allow them to run, but also
whether they run with about the same performance?

Lisa R.

From: djc (Dave Conroy)

Sent: Thursday, December 01, 1994 2:37 PM

To: 'tbr'; 'mws'; 'billz'

Cc: 'jeffm'; 'lisar'

Subject: CPU hogging

I was running a test on terp that caused lots of data cache misses in
all cylinders at the same time. What I noticed was that due to the
way everything lined up, only 1 cylinder got its cache accesses processed.
The others kept hanging around until the first cylinder finally stopped
getting cache misses. I realize that terp's timing may not be the
same as the real HW but could the real HW get into this mode also?

I realize that in "real" code the randomness of cache misses will not
normally cause this from happening but is there any requirement to
garauntee that one cylinder cannot hold off all other cylinders for
and indefinite period? There may be some algorithms (FFT's ?) that have
their data accesses line up such that each access is in a different
cache line and they may cause many successive misses before they
skip a beat and allow somebody else in.

From: tbe@MicroUnity.com

Sent: Thursday, December 01, 1994 3:17 PM

To: 'hestia'

Cc: 'glen'

Subject: minutes from final pcb review of 12/1

Following are results from the review; the first four items must be
completed before the pcb is released to fab, the other actions do not
impact the fab.

1) The "A" reference designator silkscreen on top and bottom will be mostly
obliterated by the rout line.

Action: Pattie to remove this character from both silkscreens.

2) The pcb should be released at revision 1; current marking says revision A.

Action: Pattie to correct revision marking at all locations.

3) There needs to be a clearance in the soldermask for Calliope and Euterpe
ground return under their space transformers. The via field in that ground
pad requires that the bottom soldermask also have clearances.

Action: Pattie to add same size clearances for the Ca/Eu ground pads on
both top and bottom soldermasks.

4) Fab drawing not at review, needs to be completed and checked.

Action: Glen to complete and have tbe and philip check.

5) Fab drawing not at review, needs to be completed and checked.

Action: Glen to complete and have tbe and philip check.

6) The dc-dc converter prt is still discrepant from the mechanical
criteria, which has been verified. The discrepancy is small enough to be
tolerated for the first revision.

Action: Glen to check and correct prt for the dc-dc for future use.

7) The v300p and v300m traces are routed so that one of them comes too
close to the non-plated mounting hole for the dc input connector; in
addition, the current routing forced the 3-pin relay connector to be moved
to a poor mechanical location in an attempt to maintain UL spacing.

Action: tbe to generate tkgnat that specifies the need to reassign the dc
input connector pins to allow for the proper trace routing.

8) The fan connector unregulated 12vdc ground pin is tied to the large
ground plane. It should have its own return path to the common 12vdc
ground pin at the dc-dc.

Action: At pcb assembly, drill out ground pth to open, add jumper between
connector pin and dc-dc pin. Philip to write tkgnat to ensure rework gets
done.

Tkgnat should also specify that future revisions of pcb require separate trace.

9) The Euterpe bulk bypass cap is routed between analog vdd and digital ground; there is no Calliope bulk bypass cap in the design, although one is probably needed.

Action: tbr to generate tkgnat to specify this caps deletion from the first pcb assemblies, followed by test and evaluation which will involve kludging a 1206 cap onto one of the 0805 sites for both Calliope and Euterpe. Results of test will dictate next revision pcb design and close gnat.

10) The IR receiver ground pin is connected to the large ground plane. This may or may not impair performance. Alternative is jumper or trace back to the 5vdc ground pin on the dc-dc.

Action: Yves to generate tkgnat on this to track through testing and dictate separate ground trace (if necessary) in next pcb revision.

11) An insulator needs to be added to the bottom of the Ca/Eu clamps, to mitigate risk of impairing performance or shorting to closely spaced capacitor pads, and to provide de-coupling for traces beneath the clamp.

Action: Arya to specify thickness of insulator required (assume e of 4.8)

Action: tbe to get clamps modified with bonded G10 layer of specified thickness.

12) The large capacitor at the edge of the pcb by the IR out connector is available in through-hole packaging, which would be allow for a reasonable wave solder process as well as allow for lower cost production test fixtures.

Action: Philip to generate tkgnat to ensure replacement with through-hole at next revision.

Tom Eich | tbe@microunity.com
MicroUnity Systems Engineering, Inc.|
255 Caspian Dr. Sunnyvale, CA 94089 |
(408)734-8100, (408)734-8136 fax |

From:	tbr
Sent:	Thursday, December 01, 1994 3:49 PM
To:	'paulb (Paul Berry)'
Subject:	Pandora notes
Follow Up Flag:	Follow up
Flag Status:	Red

Paul Berry wrote (on Wed Nov 30):

I've incorporated revisions you gave me regarding the Nov 17
(marketing) meeting, but I still need your corrections to my fuzzy
reporting of parts of the Nov 18 discussion that I wrote up
as "data transfer between workstation and Hestia".

I'll leave you a printout of the current set of notes, with a PostIt
yellow sticky on the part that needs your review.

I will release the notes so they appear in /u/chip/pandora/doc/notes.
(I'm finally getting to understand the 'make' and 'releasebom' procedures
well enough to release things smoothly.)
Bob Morgan has made progress in bringing up Frameviewer under
the Mosaic web browser, and I think the Pandora notes will then
be visible (in Frame format, not html) from within Mosaic.

Policy question:
I added the e-mail memo that Graham addressed to the group.

I was thinking of also adding a reduced and edited summary of yesterday's
flurry of discussion of digital video.

But please confirm: are these mail discussions things that you would like
to have incorporated into the notes file? (It seemed to me they were
a continuation of the discussion by other means and therefore should be in,
but one might argue that everyone concerned already has access to the mail,
so that inserting summaries is redundant.)

We are logging all mail to pandora to a news group, so there is a
permanent record. However, I for one have no time for reading news,
so it's certainly not as convenient. Previously, I have usually
maintained a ring binder with all the interesting email along with
other notes, but I'm not doing that in this case, and it does seem
like time to use new technology. I'd say if it's obviously a
significant follow up to something from the meetings it would make
sense to include it.

Tim

From:	tbr (Tim B. Robinson)
Sent:	Thursday, December 01, 1994 4:12 PM
To:	'mws (Mark Semmelmeyer)'
Cc:	'billz'; 'abbott'; 'djc'; 'jeffm'; 'lisar'; 'woody'
Subject:	Re: CPU hogging

Mark Semmelmeyer wrote (on Thu Dec 1):

> From djc Thu Dec 1 12:37:04 1994
>
> I was running a test on terp that caused lots of data cache misses in
> all cylinders at the same time. What I noticed was that due to the
> way everything lined up, only 1 cylinder got its cache accesses processed.
> The others kept hanging around until the first cylinder finally stopped
> getting cache misses. I realize that terp's timing may not be the
> same as the real HW but could the real HW get into this mode also?

The simualator may be not to far off. Even if it is not the same,
the hardware would probably just have a different beat pattern that
does the same thing.

> I realize that in "real" code the randomness of cache misses will not
> normally cause this from happening but is there any requirement to
> garauntee that one cylinder cannot hold off all other cylinders for
> and indefinite period? There may be some algorithms (FFT's ?) that have
> their data accesses line up such that each access is in a different
> cache line and they may cause many successive misses before they
> skip a beat and allow somebody else in.

This is a valid concern, but we have not had it as a requirement yet.
Do other multiprocessors have a similar problem?
I defer to tbr for the judgement on whether we want to put effort
into reducing this problem.

Well, I think we have been concerned all along with any inter cylinder interaction, but we
have assumed that anything that can take cache misses in the first place is of lower real
time importance. I see a possible major issue though with those parts of the real time
code that do expect to take cache misses to bring in the cache footprint anew at each time
they run. There is a potential case where a very regular pattern of accesses may occur,
with very bad consequences for other threads.

Now, isn't it the case that when a miss returns we know what thread it belongs to? I
would have thought then that we could have arranged the way the thread restarts so as to
guarantee that other waiting threads get a shot at taking a miss, since the missing thread
is presumably using it's first "load" slot to replay the missing request.

Tim

From:	woody (Jay Tomlinson)
Sent:	Thursday, December 01, 1994 4:19 PM
To:	'tbr'; 'geert'
Subject:	euterpe layout

Tim, Geert,

I will probably have trouble getting all of the layout (assigned to me) done in time for
run this weekend. I am finishing up with gtlbHzrd along with some other new logic that
needs to be added to ICC to support uncached-ifetch access (trying to help out mws).

I will give it a shot, but I just wanted to let you know that I may have trouble getting a
reasonable placement for AT done in time.

Jay

From: tbr

Sent: Thursday, December 01, 1994 4:20 PM

To: 'paulb (Paul Berry)'

Subject: Euterpe and Calliope spec sheets

Follow Up Flag: Follow up

Flag Status: Red

Paul Berry wrote (on Wed Nov 30):

> In Mouss' lunchtime talk, he mentioned that he had
> "sent the spec sheets for Euterpe and Calliope"
> to PictureTel.

> What did he send them? Can I use whatever it was
> as a prototype?

Jack Holloway did them. You should be able to get copies from him.

Tim

From:	tbr
Sent:	Thursday, December 01, 1994 4:30 PM
To:	'doi (Derek Iverson)'
Cc:	'doi'; 'gmo'; 'gregg'; 'guarino'; 'hestia'; 'iimura'; 'jeffm'; 'sandeep'; 'wayne'
Subject:	Software Bring-up Meeting - November 30, 1994
Follow Up Flag:	Follow up
Flag Status:	Red

Derek Iverson wrote (on Wed Nov 30):

Software Bringup Meeting

November 30, 1994

Item: What is dependent on SC within Euterpe? ROM & LEDs?
        Reads of cerberus registers?
Who: wayne
Status: [11/23] No progress.

All the CMOS logic is referenced to this clock. That included all the
Cerberus registers. More importantly (given where I think this
question would be comming from), is that it is used to clock counters
that control the release of reset. These are set for 1ms given
nominal (18MHz) clock rate. The reset release time will scale
linearly with the cerberus clock period. Operation sould be fine down
to DC, save for the small added delay to come out of reset.

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```
                 Software Bringup Meeting
                 ------------------------
                     November 30, 1994


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out of reset.

Tim

From:	tbr
Sent:	Thursday, December 01, 1994 4:33 PM
To:	'tbe@MicroUnity.com'
Cc:	'abbott'; 'arya'; 'graham'; 'hestia'; 'jt'
Subject:	Re: 3/4 BTSC converter
Follow Up Flag:	Follow up
Flag Status:	Red

tbe@MicroUnity.com wrote (on Wed Nov 30):

On November 29, Curtis Abbott wrote:

>Tim B. Robinson wrote (on Tue Nov 29):
>
> ...
> Unless it is out long term plan to always use a can, I would advocate
> figuring out how to use an external converter of the type used with
> some cam-corders (craig has an example). Otherwise we may find
> ourselves having to enlarge the box again just to habndle a
> contingency.
>
> Tim
>
>I believe it is rational to plan to always use a can for two reasons:
>(1) The RF modulate function is well defined, standardized, not
>subject to change, commoditized, and uses readily available analog
>signals.
>(2) The fully burdened cost (meaning including chip, chip packaging,
>power supply, heat sink, etc.) of the Euterpe cycles is much greater
>than that of the can.
>
>If Euterpe cycles were to become more numerous and 1/3 of their
>current cost, the second argument would be weakened, but the first
>would be as valid.
>
>- Curtis

I agree with your reasons, and add further (based upon our brief
conversation today) that whether or not Hestia is first deployed for analog
or digital conversion, the space and provisions for a 3/4 BTSC converter in
a can should be in the design, for reasons of upgradability and
completeness.

Even if our box were deployed for an analog only system, I have to
believe the only reasn they would choose it for that function is
becaus eit has the potential for software only upgrade to digital
operation later. Thus it would be essential to have all reaquired
hardware to support digital operation in place before deployment.

Therefore I will file a tkgnat on this and look for the results of the
converter can survey Graham mentioned for the next revision of the pcb. In
fact, I'd like to get my 2 cents in on the physical parameters of such a
can. I'm concerned about fitting it in based on particular physical

constraints such as at the rear panel more than on total pcb area.

tim

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    constraints such as at the rear panel more than on total pcb area.

tim

page from chip to geert:
Release euterpe/verilog/bsrc/iq BOM 48.0 initiated by brianl completed @ Thu Dec 1
18:13:21 PST 1994 with exit status 0.. chip

From: vo (Tom Vo)

Sent: Friday, December 02, 1994 10:22 AM

To: 'euterpe-checkins-dist'; 'lisar'; 'tbr'; 'tom'

Subject: euterpe/verilog/bsrc/xlu xlu4.obs

Update of /p/cvsroot/euterpe/verilog/bsrc/xlu
In directory merope:/N/ghidra/root/s5/vo/euterpe/verilog/bsrc/xlu

Modified Files:
    xlu4.obs
Log Message:
added gap on lhs to take care of one unrouted net .

From: lisar (Lisa Robinson)

Sent: Friday, December 02, 1994 11:42 AM

To: 'jeffm'; 'woody'

Cc: 'doi'; 'billz'; 'mws'; 'dickson'; 'tbr'; 'veena'; 'brian'

Subject: default all targets

There are now 3 new default targets in euterpe/verify/Makefile.rules
which make all of the files associated with running an individual
test. So if you need to make the files for say eventdaemotest to run
under verilog the target is

gmake allv

The other 2 targets are all and allc.
Hope I haven't missed anything.

Lisa R.


```
%.all:
        $(MAKE) $*_0.cie
        $(MAKE) $*_0.lst
        $(MAKE) $*_1.lst
        $(MAKE) $*_0.sen $*_0.srl $*_0.in $*_0.ctd $*_0.cti
        touch all

%.allc:
        $(MAKE) $*_0.cie
        $(MAKE) $*_0.lst
        $(MAKE) $*_1.lst
        $(MAKE) $*_0.sen $*_0.srl $*_0.in $*_0.ctd $*_0.cti $*_.loop
        touch allc

%.allv:
        $(MAKE) $*_V.cie
        $(MAKE) $*_V.lst
        $(MAKE) $*_1.lst
        $(MAKE) $*_V.in $*_V.ctd $*_V.cti $*_V.gmat $*_V.gmsk $*_V.gxor
        touch allv
```

From:	Curtis Abbott [abbott@tallis]
Sent:	Friday, December 02, 1994 11:46 AM
To:	'Tim B. Robinson'
Cc:	'arya@tallis'; 'graham@tallis'; 'hestia@tallis'; 'jt@tallis'; 'tbe@MicroUnity.com'
Subject:	Re: 3/4 BTSC converter

Tim B. Robinson wrote (on Thu Dec 1):

    tbe@MicroUnity.com wrote (on Wed Nov 30):

        On November 29, Curtis Abbott wrote:

        . . .
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    operation later. Thus it would be essential to have all reaquired
    hardware to support digital operation in place before deployment.

I the spirit of muddying an otherwise unequivocal opinion, I feel compelled to point out
something that occurred to me after my last posting. If we tie the "To TV" F connector to
a can sourced by baseband video and audio, we cannot configure the system to do
simultaneous watch and record. We don't have enough cycles for this anyway in any digital
video scenario, but in an analog-only application, we would.

I continue to feel that Tom's action to investigate cans is right, and Tim's point is
valid as well. I think the implication of Tim's point is that for an upgradable analog
only box, we might want to have *two* output F connectors, one labelled "To TV" and the
other "To VCR"
(the latter being fed by one of Calliope's RF outs).

What seems clear to me is that we need to have some serious pricing discussions with
potential customers for these kinds of products before we finalize board and box designs.
There are costs to upgradability; this is one example.

- Curtis

Hi ,

Two glaring violation from geert's latest euterpe placement :

1. from the xlu output ff to rg ff .

ff + ef + buf + mux5 + mux2ff (the ef drives some 3mm worth of wire)

|-xlu---|-------rg----------|

Part of the problem is due to stale timing number from the xlu sc cell (old rcode) . I
vaguely remembered tbr getting an OK pest report on this path a while back . Has this
path changed since then ? I know we picked up an extra .5mm of wire from
shrinking the gap in the middle of the xlu to 0 .

2. From dr to drio .

We have some 9 mm of wire to drive (some 500ps of rc delay) .
I'm told that this is a 100Mhz path . But topt is seeing
it as a 1GHz path .

tvo

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>
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>discussions with potential customers for these kinds of products before
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```
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>
>- Curtis
```

Am I missing something here? The 3/4 converter can will be behind the Calliope controlled
bypass relay (from the outside world), and therefore analog input Hestia could pass the
entire spectrum to a vcr, which can tune and record while passing the spectrum on to a TV,
where the user can tune at will. Since you say that the concern you raise is moot for
digital Hestia, I only address the analog input scenario here, which I assume is no
different from my setup at home, where the cable box feeds the vcr which feeds the TV.

Re-reading the Toltek spec 2.14 RF bypass, it says that the digital terminal must be
equipped with the ability to pass analog signals through to any cable ready electronics,
and that this ability must be configurable by the subscriber, using the EPG/N to allow
this so-called auto bypass, whether on or off. The only concern I see here is that when
Hestia is in sleep mode it can meet this requirement.

-Tom

Tom Eich	tbe@microunity.com
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255 Caspian Dr. Sunnyvale, CA 94089	
(408)734-8100, (408)734-8136 fax	

From:	tbr (Tim B. Robinson)
Sent:	Friday, December 02, 1994 3:26 PM
To:	'vo (Tom Vo)'
Cc:	'billz (Bill Zuravleff)'; 'geert (Geert Rosseel)'
Subject:	timing paths

Tom Vo wrote (on Fri Dec 2):

   Hi ,

   Two glaring violation from geert's latest euterpe placement :

   1. from the xlu output ff to rg ff .

   ff + ef + buf + mux5 + mux2ff (the ef drives some 3mm worth of wire)

   |-xlu---|-------rg----------|

   Part of the problem is due to stale timing number
   from the xlu sc cell (old rcode) . I vaguely remembered tbr
   getting an OK pest report on this path a while back . Has this path
   changed since then ? I know we picked up an extra .5mm of wire from
   shrinking the gap in the middle of the xlu to 0 .

I did get an OK pest report (somewhat to my surprise, though I recall it was checked out
as OK. We have to have the 2 mux levels (that's the main bypass mux. The problem is the
buf, which is only there because the XLU has a ***NON STANDARD*** output. As I recall
from pest, the 3mm was not long enough for the ef to be effective in getting back the
delay of the buffer.

   2. From dr to drio .

   We have some 9 mm of wire to drive (some 500ps of rc delay) .
   I'm told that this is a 100Mhz path . But topt is seeing
   it as a 1GHz path .

To the extent that we need good skew control (< 1ns) at the interface, this is a 1GHz
path. However, latency could perhaps be relaxed without too major an impact (ie more
staging) - bill would have to comment on what it takes to do that. How doe we come to
have an obviously impossible 9mm path? I thought this had been looked at and passed as OK
as a flop -> flop path.

Tim

From: woody (Jay Tomlinson)

Sent: Friday, December 02, 1994 5:06 PM

To: 'tbr'

Cc: 'billz'; 'mws'; 'dickson'

Subject: ram array hazards/conflicts

Tim,
I checked with Billz. He indicated that hz has been updated, but euterpe.V may
not have been. Rich indicated that he updated euterpe.V and just left the extra
outputs floating. Mark will connect to these signals when he gets uu updated.

Jay

From: tom (Tom Laidig)

Sent: Friday, December 02, 1994 7:15 PM

To: 'geert (Geert Rosseel)'

Cc: 'tom (Thomas Laidig)'; 'tbr (Tim B. Robinson)'; 'lisar (Lisa Robinson)'; 'Tom Vo'; 'Kurt Wampler'; 'Mark Hofmann'

Subject: euterpe build

As I understand, you're planning to attempt a full-chip P&R of euterpe
over the weekend, in the snapshot area. I strongly suggest that you
use the new .pdl files that are being generated now in /u/chip.

It seems that the proper course would be to build the leafcell layouts
and then the .pdl files in the snapshot area, but this would delay the
use of these .pdls for a couple days. So, I suggest we do the
following: cp the .pdls from /u/chip after they're done (when `chipq'
no longer lists job # 2212, a build in proteus/gards); then (when cpu
time is relatively available) do a getbom and build of leafcell layouts
in the snapshot; then rebuild the .pdls in the snapshot.

Comments?

```
--
  ooooO  Ooooo
 (  _)  (_  )
 \(  tau  )/
  ()    ()
```

From:	tbr
Sent:	Friday, December 02, 1994 7:19 PM
To:	'woody (Jay Tomlinson)'
Cc:	'billz'; 'dickson'; 'mws'
Subject:	ram array hazards/conflicts
Follow Up Flag:	Follow up
Flag Status:	Red

Jay Tomlinson wrote (on Fri Dec 2):

Tim,
I checked with Billz. He indicated that hz has been updated, but euterpe.V may
not have been. Rich indicated that he updated euterpe.V and just left the extra
outputs floating. Mark will connect to these signals when he gets uu updated.

Thanks
Tim

From:	tbr
Sent:	Friday, December 02, 1994 7:28 PM
To:	'tom (Tom Laidig)'
Cc:	'geert (Geert Rosseel)'; 'hopper (Mark Hofmann)'; 'lisar (Lisa Robinson)'; 'Thomas Laidig'; 'Tom Vo'; 'Kurt Wampler'
Subject:	euterpe build
Follow Up Flag:	Follow up
Flag Status:	Red

Tom Laidig wrote (on Fri Dec 2):

As I understand, you're planning to attempt a full-chip P&R of euterpe
over the weekend, in the snapshot area. I strongly suggest that you
use the new .pdl files that are being generated now in /u/chip.

It seems that the proper course would be to build the leafcell layouts
and then the .pdl files in the snapshot area, but this would delay the
use of these .pdls for a couple days. So, I suggest we do the
following: cp the .pdls from /u/chip after they're done (when `chipq'
no longer lists job # 2212, a build in proteus/gards); then (when cpu
time is relatively available) do a getbom and build of leafcell layouts
in the snapshot; then rebuild the .pdls in the snapshot.

Comments?

I'd like to resist doing any cheating in the snapshot. Up to this
point we have been careful to make all changes by getting a bom and
running the make. This big run will certainly not be the last
so unless we thing the changes wouldmake or break it, my preference
woud be to "do it right".

Tim

From: tbr

Sent: Saturday, December 03, 1994 2:11 PM

To: 'doi'

Subject: getbom

Follow Up Flag: Follow up

Flag Status: Red

I have been seeing a bunch of messages like:

13.4   p611_etest_1x10_pmosma.ly   (Evict No)
Warning: /n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_pmosma.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_pmosma.ly.No - (status 16)

which I have not seen before. What are they trying to tell me?

Tim

/

From:	Geert Rosseel [geert@rhea]
Sent:	Saturday, December 03, 1994 2:13 PM
To:	'geert@rhea'
Subject:	pager log, sender copy

```
page from geert to geert:
pageme gmake geert_euterpegards start:Dec_03_10:11 end: Dec_03_12:12 exit
1
```

From:	tbr
Sent:	Saturday, December 03, 1994 5:21 PM
To:	'doi'
Cc:	'geert'
Subject:	getbom
Follow Up Flag:	Follow up
Flag Status:	Red

The new getbom in the snapshot proteus came up with some warnings
which i don't understand, though there's probably a good explanation:

WARNING SUMMARY --------------------------------
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "ad16.ly" needs to be evicted (same name as a file that is being
extracted) - moving to .#ad16.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "ad16st1.ly" needs to be evicted (same name as a file that is being
extracted) - moving to .#ad16st1.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "ad16st2.ly" needs to be evicted (same name as a file that is being
extracted) - moving to .#ad16st2.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "latchx1.ly" needs to be evicted (same name as a file that is being
extracted) - moving to .#latchx1.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "locked-cells" needs to be evicted (same name as a file that is being
extracted) - moving to .#locked-cells.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mosne_25xp45.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#mosne_25xp45.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mosne_25xp95_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#mosne_25xp95_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mosne_25xp95_p45drn.ly" needs to be evicted (same name as a file
that is being extracted) - moving to .#mosne_25xp95_p45drn.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mosne_2xp95_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#mosne_2xp95_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_25x2p0_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#mospe_25x2p0_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_25xp45.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#mospe_25xp45.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_25xp5_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#mospe_25xp5_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_25xp95_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#mospe_25xp95_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_25xp95_p45drn.ly" needs to be evicted (same name as a file
that is being extracted) - moving to .#mospe_25xp95_p45drn.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_2xp95_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#mospe_2xp95_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospp_25x2p0_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#mospp_25x2p0_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nf_25x2p0_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#nf_25x2p0_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nf_25xp5_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#nf_25xp5_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nfc_25x1p5_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#nfc_25x1p5_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nfc_25x2p0_f.ly" needs to be evicted (same name as a file that is
being extracted) - moving to .#nfc_25x2p0_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "npolysc_f.ly" needs to be evicted (same name as a file that is being

extracted) - moving to .#npolysc_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nsas_f.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#nsas_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nsdecendcap_2udr.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#nsdecendcap_2udr.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nsp_f.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#nsp_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_bjt1b.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_bjt1b.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_cstring1a.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_cstring1a.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_cstring1b.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_cstring1b.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_nmos1b.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_nmos1b.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_nmos2b.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_nmos2b.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_nmos3b.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_nmos3b.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_pmos2a.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_pmos2a.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_pmos2b.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_pmos2b.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_pmosma.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_pmosma.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "pad_1x10a.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#pad_1x10a.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "pad_1x10b.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#pad_1x10b.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "pf_25x2p0_f.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#pf_25x2p0_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "pf_25xp5_f.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#pf_25xp5_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "ppolysc_f.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#ppolysc_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "psp_f.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#psp_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "rotated_nmos1_f.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#rotated_nmos1_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "rotated_nmos2_f.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#rotated_nmos2_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "rotated_pmos1_f.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#rotated_pmos1_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "rotated_pmos2_f.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#rotated_pmos2_f.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "subscontfilsca.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#subscontfilsca.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "subscontfilscb.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#subscontfilscb.ly.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "vlsi.cko" needs to be evicted (same name as a file that is being extracted) - moving to .#vlsi.cko.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "vlsi.log" needs to be evicted (same name as a file that is being extracted) - moving to .#vlsi.log.No - (status 16)

/n/auspex/s23/euterpe-proteus-cp/ged: File "Makefile" needs to be evicted (same name as a file that is being extracted) - moving to .#Makefile.No - (status 16)

At least in the case of the last file, I diffed it with the version
that was actually extracted and it's identical.

Tim

From:	tbr (Tim B. Robinson)
Sent:	Saturday, December 03, 1994 5:21 PM
To:	'doi'
Cc:	'geert'
Subject:	getbom

The new getbom in the snapshot proteus came up with some warnings which i don't
understand, though there's probably a good explanation:

```
WARNING SUMMARY -------------------------------
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "ad16.ly" needs to be evicted (same
name as a file that is being extracted) - moving to .#ad16.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "ad16st1.ly" needs to be evicted
(same name as a file that is being extracted) - moving to .#ad16st1.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "ad16st2.ly" needs to be evicted
(same name as a file that is being extracted) - moving to .#ad16st2.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "latchx1.ly" needs to be evicted
(same name as a file that is being extracted) - moving to .#latchx1.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "locked-cells"
needs to be evicted (same name as a file that is being extracted) - moving to .#locked-
cells.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mosne_25xp45.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#mosne_
25xp45.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mosne_25xp95_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#mosne_
25xp95_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mosne_25xp95_p45drn.ly" needs to
be evicted (same name as a file that is being extracted) - moving to .#mosne_25xp95
_p45drn.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mosne_2xp95_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#mosne_
2xp95_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_25x2p0_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#mospe_
25x2p0_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_25xp45.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#mospe_
25xp45.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_25xp5_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#mospe_
25xp5_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_25xp95_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#mospe_
25xp95_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_25xp95_p45drn.ly" needs to
be evicted (same name as a file that is being extracted) - moving to .#mospe_25xp95
_p45drn.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospe_2xp95_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#mospe_
2xp95_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "mospp_25x2p0_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#mospp_
25x2p0_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nf_25x2p0_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#nf_25x2p0
_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nf_25xp5_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#nf_25xp5
_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nfc_25x1p5_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#nfc_25x1p5
_f.ly.No - (status 16)
```

/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nfc_25x2p0_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#nfc_25x2p0
_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "npolysc_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .
#npolysc_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nsas_f.ly" needs to be evicted
(same name as a file that is being extracted) - moving to .#nsas_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nsdecendcap_2udr.ly" needs to be
evicted (same name as a file that is being extracted) - moving to .#nsdecendcap_2udr.ly.No
- (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "nsp_f.ly" needs to be evicted
(same name as a file that is being extracted) - moving to .#nsp_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_bjt1b.ly" needs to
be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10
_bjt1b.ly.No - (status
16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_cstring1a.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#p611
_etest_1x10_cstring1a.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_cstring1b.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#p611
_etest_1x10_cstring1b.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_nmos1b.ly" needs
to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10
_nmos1b.ly.No - (status
16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_nmos2b.ly" needs
to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10
_nmos2b.ly.No - (status
16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_nmos3b.ly" needs
to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10
_nmos3b.ly.No - (status
16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_pmos2a.ly" needs
to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10
_pmos2a.ly.No - (status
16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_pmos2b.ly" needs
to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10
_pmos2b.ly.No - (status
16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_pmosma.ly" needs
to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10
_pmosma.ly.No - (status
16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "pad_1x10a.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#pad_
1x10a.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "pad_1x10b.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#pad_
1x10b.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "pf_25x2p0_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#pf_25x2p0
_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "pf_25xp5_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .#pf_25xp5
_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "ppolysc_f.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .
#ppolysc_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "psp_f.ly" needs to be evicted
(same name as a file that is being extracted) - moving to .#psp_f.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "rotated_nmos1_f.ly" needs to be
evicted (same name as a file that is being extracted) - moving to .#rotated_nmos1_f.ly.No
- (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "rotated_nmos2_f.ly" needs to be

evicted (same name as a file that is being extracted) - moving to .#rotated_nmos2_f.ly.No
- (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "rotated_pmos1_f.ly" needs to be
evicted (same name as a file that is being extracted) - moving to .#rotated_pmos1_f.ly.No
- (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "rotated_pmos2_f.ly" needs to be
evicted (same name as a file that is being extracted) - moving to .#rotated_pmos2_f.ly.No
- (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "subscontfilsca.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .
#subscontfilsca.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "subscontfilscb.ly"
needs to be evicted (same name as a file that is being extracted) - moving to .
#subscontfilscb.ly.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "vlsi.cko" needs to be evicted
(same name as a file that is being extracted) - moving to .#vlsi.cko.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "vlsi.log" needs to be evicted
(same name as a file that is being extracted) - moving to .#vlsi.log.No - (status 16)
/n/auspex/s23/euterpe-proteus-cp/ged: File "Makefile" needs to be evicted (same name as a
file that is being extracted) - moving to .#Makefile.No - (status 16)

At least in the case of the last file, I diffed it with the version that was actually
extracted and it's identical.

Tim

From:	Geert Rosseel [geert@rhea]
Sent:	Saturday, December 03, 1994 8:43 PM
To:	'geert@rhea'
Subject:	pager log message

```
page from geert to geert:
pageme gmake gards/geert_euterpe-iter.garout.lis start:Dec_03_13:32 end:
Dec_03_18:41 exit 0
```

From:	tbr
Sent:	Saturday, December 03, 1994 9:24 PM
To:	'Curtis Abbott'
Cc:	'craig@tallis'; 'dickson@tallis'
Subject:	esum
Follow Up Flag:	Follow up
Flag Status:	Red

Curtis Abbott wrote (on Tue Nov 15):

> I've gone around most people in my group and couldn't find any ardent
> lovers of esum. It replaces about 15 instructions, so if there's a
> need for it, it'll definitely be a win. People like it, but they're
> not using it and don't have specific ideas about how they would.
>
> I'd say if it'll make tapeout happen sooner, you can get rid of it.

It's still in, and it does not look like another sacrificial offering
will be needed, at least not in the datapath.

Tim

From:	Tim B. Robinson [tbr@tallis]
Sent:	Saturday, December 03, 1994 9:24 PM
To:	'Curtis Abbott'
Cc:	'craig@tallis'; 'dickson@tallis'
Subject:	esum

Curtis Abbott wrote (on Tue Nov 15):

> I've gone around most people in my group and couldn't find any ardent
> lovers of esum. It replaces about 15 instructions, so if there's a
> need for it, it'll definitely be a win. People like it, but they're
> not using it and don't have specific ideas about how they would.
>
> I'd say if it'll make tapeout happen sooner, you can get rid of it.

It's still in, and it does not look like another sacrificial offering will be needed, at
least not in the datapath.

Tim

From: tbr

Sent: Saturday, December 03, 1994 10:44 PM

To: 'geert'

Subject: lvs netlist

Follow Up Flag: Follow up

Flag Status: Red

I have been trying to make a new .splvs netlist (for csyn) after
updating to the latest BOM and something in the Makefile had\s
changes, such that it now thinks it has no rule. I've been peeling it
back, and it appears to be the step:

tbr@gamorra ~/euterpe/verilog/bsrc 437 % make gards/tbr_euterpe-pass1.sdl
gmake: *** No rule to make target `gards/tbr_euterpe-pass1.sdl'. Stop.

which is causing the problem. Any idea what changed?

Tim

From: tbr (Tim B. Robinson)
Sent: Saturday, December 03, 1994 10:45 PM
To: 'geert'
Subject: lvs netlist

I have been trying to make a new .splvs netlist (for csyn) after updating to the latest
BOM and something in the Makefile had\s changes, such that it now thinks it has no rule.
I've been peeling it back, and it appears to be the step:

```
tbr@gamorra ~/euterpe/verilog/bsrc 437 % make gards/tbr_euterpe-pass1.sdl
gmake: *** No rule to make target `gards/tbr_euterpe-pass1.sdl'.  Stop.
```

which is causing the problem. Any idea what changed?

Tim

From:	tbr
Sent:	Saturday, December 03, 1994 10:49 PM
To:	'geert'
Subject:	lvs problem
Follow Up Flag:	Follow up
Flag Status:	Red

I think the problem may be that there is some new file in a
sub-directory you are expecting. My Makefile.tst only includes the ck
section.
I just tried to rebuild it and that one fails with:

Memory usage: 0.250MB
/usr/local/bin/perl genpim.pl > pim.tmp
mv pim.tmp gards/ck-pass1.pim
#
Get an initial sdl file. A manhattan approximation will be used
#
gmake CYCLETIME=895 gards/ck-pass2.sdl
gmake[2]: Entering directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/ck'
gmake[2]: *** No rule to make target `gards/ck-pass2.sdl'. Stop.
gmake[2]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/ck'
gmake[1]: *** [ck-base.short.nets] Error 1
gmake[1]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/ck'
gmake: *** [ckgards] Error 1

Tim

From:	tbr (Tim B. Robinson)
Sent:	Saturday, December 03, 1994 10:49 PM
To:	'geert'
Subject:	lvs problem

I think the problem may be that there is some new file in a sub-directory you are
expecting. My Makefile.tst only includes the ck section.
I just tried to rebuild it and that one fails with:

```
Memory usage: 0.250MB
/usr/local/bin/perl genpim.pl > pim.tmp
mv pim.tmp gards/ck-pass1.pim
#
# Get an initial sdl file.  A manhattan approximation will be used # gmake  CYCLETIME=895
gards/ck-pass2.sdl
gmake[2]: Entering directory
`/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/ck'
gmake[2]: *** No rule to make target `gards/ck-pass2.sdl'.  Stop.
gmake[2]: Leaving directory
`/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/ck'
gmake[1]: *** [ck-base.short.nets] Error 1
gmake[1]: Leaving directory
`/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/ck'
gmake: *** [ckgards] Error 1
```

Tim

From: woody (Jay Tomlinson)

Sent: Sunday, December 04, 1994 1:14 AM

To: 'tbr (Tim B. Robinson)'

Subject: bad port

Tim B. Robinson wrote (on Sat Dec 3):

I have been trying to get a new .splvs netlist and v2e reports:

(?V2E) ***WARNING*** Unsupported connection on Port "1" of instance "UzCEifePgSzSel1_abm" of module "c01_4" : Unconnected bits in vector ports not supported.

Can you check out what might be wrong here?

Tim

Only 3 bits were connected to a port that was expecting 4 bits. also _N ports
did not have any connection. I guess v2e does like that.

I fixed euterpe.V and checked it in.
Jay

From:	tbr
Sent:	Sunday, December 04, 1994 1:24 AM
To:	'woody (Jay Tomlinson)'
Subject:	bad port
Follow Up Flag:	Follow up
Flag Status:	Red

Jay Tomlinson wrote (on Sat Dec 3):

Tim B. Robinson wrote (on Sat Dec 3):

I have been trying to get a new .splvs netlist and v2e reports:

(?V2E) ***WARNING*** Unsupported connection on Port "1" of instance "UzCEifePgSzSel1_abm" of module "c01_4" : Unconnected bits in vector ports not supported.

Can you check out what might be wrong here?

Tim

Only 3 bits were connected to a port that was expecting 4 bits. also _N ports
did not have any connection. I guess v2e does like that.

I fixed euterpe.V and checked it in.
 Jay
Thanks.

Tim

The following differences were noticed since Yesterday.
in /n/auspex/s24/solo/test/compass/vlsi.boo and check.list

CELLNAME iobyte
35c35
< /u/chip/euterpe/proteus/compass/layouts/ioffout.ly   1.9   Dec 4 11:49:43 1994

> /u/chip/euterpe/proteus/compass/layouts/ioffout.ly   1.8   May 20 07:39:21 1994
57c57,59
< /u/chip/euterpe/proteus/compass/layouts/latchx1.ly   1.12   Dec 4 11:49:49 1994

> /u/chip/euterpe/proteus/compass/layouts/isrc_lobe.ly   1.9   Dec 1 15:00:08 1994
> /u/chip/euterpe/proteus/compass/layouts/latchx1.ly   1.10   May 7 01:04:54 1994
> latchx1.ly   Mismatch RCS = 1.11 release = 1.10
88a91
> /u/chip/euterpe/proteus/compass/layouts/pld_lobe.ly   1.7   Mar 7 10:10:37 1994

....
The following mismatches were found between the released Version
cell or sub cells and the Version found in RCS.
You may want to release the later version, maybe not.

....
The following layouts were run today. This means either a change in
the schematic or layout.

Lvslog:12/04/94 GMT ***running LVS from echidna pid 17245
Lvslog:12/04/94 GMT ***/n/auspex/s24/solo/test
Lvslog:12/04/94 GMT ***running LVS from abderus pid 6759
Lvslog:12/04/94 GMT ***/n/auspex/s24/solo/test
Lvslog:12/04/94 20:39 GMT running lvs -drac L iobyte vs S iobyte
Drclog:12/04/94 GMT ***running DRC from echidna pid 15299
Drclog:12/04/94 GMT ***/n/auspex/s24/solo/test
Drclog:12/04/94 GMT ***running DRC from abderus pid 4778
Drclog:12/04/94 GMT ***/n/auspex/s24/solo/test
Drclog:12/04/94 20:14 GMT running DRC -drac   on iobyte

....
The following cells may have bad lvs results. Check it out.

.....Circuit DISCREPANCIES

Verify/pl_euh/pl_euh.compare/pl_euh.lvs

.....Possible Pin Problems

pl_eus pins may not match

....
The following cells may have bad drc results. Check it out.

☐ ************ERROR pl_euh FAILED DRC DIFF
☐ ************ERROR pl_eus FAILED DRC DIFF

....
The following cells may have shorts or opens.

From:	tbr
Sent:	Monday, December 05, 1994 8:33 AM
To:	'fwo'
Cc:	'geert'; 'dickson'; 'hopper'
Subject:	csyn
Follow Up Flag:	Follow up
Flag Status:	Red

Withe the latest csyn and BOM 187.1 there are new errors (including
illegal leaf cell pin names). The output is in
~tbr/euterpe/verilog/bsrc/tbr_euterpe-pass1.csyn

Tim

From:	tbr (Tim B. Robinson)
Sent:	Monday, December 05, 1994 8:33 AM
To:	'fwo'
Cc:	'geert'; 'dickson'; 'hopper'
Subject:	csyn

Withe the latest csyn and BOM 187.1 there are new errors (including illegal leaf cell pin names). The output is in ~tbr/euterpe/verilog/bsrc/tbr_euterpe-pass1.csyn

Tim

From: solo (John Campbell)

Sent: Monday, December 05, 1994 9:38 AM

To: 'hopper (Mark Hofmann)'; 'tbr (Tim B. Robinson)'

Subject: VerifyRun (fwd)

i guess i just put you two on /u/chip and not on snapshot. there are
two separate verify runs that fire off. not the dirname as
/n/auspex/s24/solo/snap/compass/vlsi.boo on this one. i will add you
for a few days till the dust settles again and you scream for me to stop.

as John Campbell was saying ....
..Subject: VerifyRun
..Cc: lisar, tom, vo

..
..The following differences were noticed since Yesterday.
..in /n/auspex/s24/solo/snap/compass/vlsi.boo and check.list
..--

..
..---------------------
..CELLNAME pl_euh
..131,133c131,133
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbbufdh16s.ly No   4-Dec-94 6:57:49 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbcmos2ecldf2s.ly No   4-Dec-94 21:09:51 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbcmos2ecldf6s.ly No   4-Dec-94 12:20:47 GMT
..---
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbbufdh16s.ly No   6-Nov-94 5:28:07 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbcmos2ecldf2s.ly No   6-Nov-94 12:09:33 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbcmos2ecldf6s.ly No   6-Nov-94 12:33:02 GMT
..150,155c150,155
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff2df16s.ly No   4-Dec-94 19:25:07 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff4df12s.ly No   4-Dec-94 16:42:02 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff4dh16s.ly No   4-Dec-94 9:26:09 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff5df8s.ly No   4-Dec-94 9:57:06 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff6df8s.ly No   4-Dec-94 16:22:15 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborffb7df8s.ly No   4-Dec-94 10:06:48 GMT
..---
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff2df16s.ly No   6-Nov-94 10:06:22 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff4df12s.ly No   6-Nov-94 9:51:57 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff4dh16s.ly No   6-Nov-94 7:59:06 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff5df8s.ly No   6-Nov-94 9:11:21 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff6df8s.ly No   6-Nov-94 9:38:13 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborffb7df8s.ly No   6-Nov-94 10:09:35 GMT

..---------------------
..CELLNAME pl_eus
..137,139c137,139
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbbufdh16s.ly No   4-Dec-94 6:57:49 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbcmos2ecldf2s.ly No   4-Dec-94 21:09:51 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbcmos2ecldf6s.ly No   4-Dec-94 12:20:47 GMT
..---
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbbufdh16s.ly No   6-Nov-94 5:28:07 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbcmos2ecldf2s.ly No   6-Nov-94 12:09:33 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xbcmos2ecldf6s.ly No   6-Nov-94 12:33:02 GMT
..156,161c156,161
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff2df32s.ly No   4-Dec-94 10:55:27 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff4df12s.ly No   4-Dec-94 16:42:02 GMT

```
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff4dh16s.ly No    4-Dec-94 9:26:09 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff5df8s.ly No    4-Dec-94 9:57:06 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff6df8s.ly No    4-Dec-94 16:22:15 GMT
..< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborffb7df8s.ly No    4-Dec-94 10:06:48 GMT
..---
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff2df32s.ly No    6-Nov-94 9:55:07 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff4df12s.ly No    6-Nov-94 9:51:57 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff4dh16s.ly No    6-Nov-94 7:59:06 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff5df8s.ly No    6-Nov-94 9:11:21 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborff6df8s.ly No    6-Nov-94 9:38:13 GMT
..> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/leaf/xborffb7df8s.ly No    6-Nov-94 10:09:35 GMT
```

..--------------------
..CELLNAME iobyte
..36d35
..< ioffout.ly   Mismatch RCS = 1.9 release = 1.8
..60c59
..< latchx1.ly   Mismatch RCS = 1.12 release = 1.10
..---
..> latchx1.ly   Mismatch RCS = 1.11 release = 1.10
..

....
..The following mismatches were found between the released Version
..cell or sub cells and the Version found in RCS.
..You may want to release the later version, maybe not.
..
..ioffout.ly   Mismatch RCS = 1.9 release = 1.8
..latchx1.ly   Mismatch RCS = 1.12 release = 1.10
..

....
..The following layouts were run today. This means either a change in
..the schematic or layout.
..
..Lvslog:12/05/94 GMT ***running LVS from echidna pid 26999
..Lvslog:12/05/94 GMT ***/n/auspex/s24/solo/snap
..Lvslog:12/05/94 05:06 GMT running lvs -drac L pl_euh vs   S pl_euh
..Lvslog:12/05/94 05:08 GMT running lvs -drac L pl_eus vs   S pl_eus
..Drclog:12/05/94 GMT ***running DRC from echidna pid 24929
..Drclog:12/05/94 GMT ***/n/auspex/s24/solo/snap
..Drclog:12/05/94 04:46 GMT running DRC -drac   on pl_euh
..Drclog:12/05/94 04:47 GMT running DRC -drac   on pl_eus
..Drclog:12/05/94 04:51 GMT running DRC -drac   on iobyte
..

....
..The following cells may have bad lvs results. Check it out.
..
.......Circuit DISCREPANCIES
..
..
.......Possible Pin Problems
..
..pl_euh pins may not match
..pl_eus pins may not match
..scsof1 pins may not match
..scsdm8bv3 pins may not match
..scsdm16 pins may not match
..scxbcgbfr0 pins may not match
..

....
..The following cells may have bad drc results. Check it out.
..
..□ ***********ERROR pl_euh FAILED DRC DIFF

..☐ ************ERROR pl_eus FAILED DRC DIFF
..☐ ************ERROR iobyte FAILED DRC DIFF
..

....
..The following cells may have shorts or opens.
..

....
regards,
solo a.k.a. John Campbell   x516

From: doi (Derek Iverson)

Sent: Monday, December 05, 1994 10:20 AM

To: 'tbr (Tim B. Robinson)'

Subject: getbom

Tim B. Robinson writes:
>
> I have been seeing a bunch of messages like:
>
> 13.4   p611_etest_1x10_pmosma.ly   (Evict No)
> Warning: /n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_pmosma.ly" needs to be evicted
(same name as a file that is being extracted) - moving to .#p611_etest_1x10_pmosma.ly.No - (status 16)
>
> which I have not seen before. What are they trying to tell me?

This means that the file in question is found locally but there is
no mention of it in the CVS/Entries file. CVS will not extract a file
is it finds a 'normal' file (not under CVS control) by the same
name as the one being extracted.

Does this make sense?

doi

From: geert (Geert Rosseel)

Sent: Monday, December 05, 1994 10:50 AM

To: 'wampler'

Cc: 'hopper'; 'tbr'; 'vo'

Subject: New GARDS limit

I get this :

FILES FOR THIS ENTIRE RUN:
  DESIGN_FILE: chip_euterpe-iter.dff
  LISTING: chip_euterpe-iter.garout.lis
  CONGVAL: padobs.cvp
  STRATEGY: chip_euterpe-iter.rcf
** GAROUT error: 67

At position 57 in line 10 of the RCF file, the number 400 is out of the
allowed range of values for the indicated parameter (0 to 99).

Severity 7 is fatal.

*** ERROR   67 IN RSTRAT ***   SEVERITY 7

The line it flags is :

 control: netlist=dcache.nets; f(netflag)=-1; passes=2;
linesearch: searchdepth = 6; first_layer=2; best = 400; pinpairlimit = -3;
linesearch: searchdepth = 40; first_layer=2; best = 400; pinpairlimit = -3;

l am pretty sure this used to work with the previous version of GARDS.

                 Geert

From: tbr

Sent: Monday, December 05, 1994 10:54 AM

To: 'doi (Derek Iverson)'

Subject: getbom

Follow Up Flag: Follow up

Flag Status: Red

Derek Iverson wrote (on Mon Dec 5):

   Tim B. Robinson writes:
   >
   > I have been seeing a bunch of messages like:
   >
   > 13.4   p611_etest_1x10_pmosma.ly   (Evict No)
   > Warning: /n/auspex/s23/euterpe-proteus-cp/compass/layouts: File "p611_etest_1x10_pmosma.ly" needs to be evicted (same name as a file that is being extracted) - moving to .#p611_etest_1x10_pmosma.ly.No - (status 16)
   >
   > which I have not seen before. What are they trying to tell me?

   This means that the file in question is found locally but there is
   no mention of it in the CVS/Entries file. CVS will not extract a file
   is it finds a `normal' file (not under CVS control) by the same
   name as the one being extracted.

   Does this make sense?

Maybe. What had happened was that I had done a getbom as tbr, rather
than chip. I then did a find to rm all the files owned by me. All
sorts of stuff got removed, and I think that may have included the
CVS/Enrtires file in some cases.

Tim

```
Geert writes:
------------
>I get this :
>
>FILES FOR THIS ENTIRE RUN:
>    DESIGN_FILE:   chip_euterpe-iter.dff
>    LISTING:       chip_euterpe-iter.garout.lis
>    CONGVAL:       padobs.cvp
>    STRATEGY:      chip_euterpe-iter.rcf
> ** GAROUT error: 67
>
> At position 57 in line 10 of the RCF file, the number 400 is out of
> the allowed range of values for the indicated parameter (0 to 99).
>
> Severity 7 is fatal.
>
> *** ERROR    67 IN RSTRAT    ***     SEVERITY  7
>
>The line it flags is :
>
> control: netlist=dcache.nets; f(netflag)=-1; passes=2;
>linesearch: searchdepth = 6;   first_layer=2;   best = 400; pinpairlimit
>=
-3;
>linesearch: searchdepth = 40; first_layer=2; best = 400; pinpairlimit =
-3;
>
>
>I am pretty sure this used to work with the previous version of GARDS.

  The current reference manual states that the bestescape parameter can be no
  greater than 99.  I can confirm that it was limited to 99 in the previous
  version of GAROUT, having bumped into it myself.

  - Kurt
```

From: tom (Tom Laidig)

Sent: Monday, December 05, 1994 11:31 AM

To: 'tbr (Tim B. Robinson)'; 'brianl (Brian Lee)'

Subject: lpe mail

Chip received the attached mail as a result of running lpe on the leaf
lobes (this is from the snapshot build that was running over the
weekend). Unless there was some problem, I assume this mail can be
flushed.

```
--
   ooooO  Ooooo
   (_) (_)
   \( tau )/
   ()  ()
```

>From chip Sun Dec 4 13:45:39 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14424; Sun, 4 Dec 1994 13:45:39 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16164; Sun, 4 Dec 1994 13:45:35 -0800
Date: Sun, 4 Dec 1994 13:45:35 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042145.NAA16164@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: OR

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:45:35 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16160; Sun, 4 Dec 1994 13:45:34 -0800
Date: Sun, 4 Dec 1994 13:45:34 -0800
From: root (Charlie Root)
Message-Id: <199412042145.NAA16160@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: buf1x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: buf1x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4

ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                     *
*        IIIIIII  SSSSSS   SSSSSS            *
*          I    S    S            *
*          I    S    S            *
*          I    SSSSS   SSSSS               *
*          I      S    S         *
*          I      S    S         *
*        IIIIIII  SSSSSS   SSSSSS            *
*                                     *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:45:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c buf1x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 16061.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& buf1x1.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2   7/21/94
        lsh: 2.4.15   8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

        vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
        TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
        TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
        TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
        TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:

TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
        TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary         *
grep: BUF1X1.cmpsum: No such file or directory
grep: BUF1X1.cmpsum: No such file or directory
*******************************************
```

```
*******************************************
*******************************************
**                              **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**       PLEASE LOOK IN BUF1X1.err      **
**                              **
*******************************************
*******************************************
```

cat buf1x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/buf1x1.compare_lpe/buf1x1.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 13:47:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14463; Sun, 4 Dec 1994 13:47:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16277; Sun, 4 Dec 1994 13:47:31 -0800
Date: Sun, 4 Dec 1994 13:47:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042147.NAA16277@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:47:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16273; Sun, 4 Dec 1994 13:47:31 -0800
Date: Sun, 4 Dec 1994 13:47:31 -0800
From: root (Charlie Root)
Message-Id: <199412042147.NAA16273@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: buf1x2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe

Current Layout: buf1x2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/********************************************************************/
*                                    *
*       IIIIII  SSSSSS  SSSSSS              *
*         I    S    S              *
*         I    S    S              *
*         I     SSSSS   SSSSS             *
*         I        S   S          *
*         I        S   S          *
*       IIIIII  SSSSSS  SSSSSS              *
*                                    *
/********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:47:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c buf1x2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 16174.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& buf1x2.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2   7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

        vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
        TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
        TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: BUF1X2.cmpsum: No such file or directory
grep: BUF1X2.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                      **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN BUF1X2.err       **
**                      **
*******************************************
*******************************************
```

cat buf1x2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/buf1x2.compare_lpe/buf1x2.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 13:48:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id NAA14471; Sun, 4 Dec 1994 13:48:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA16390; Sun, 4 Dec 1994 13:48:33 -0800
Date: Sun, 4 Dec 1994 13:48:33 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042148.NAA16390@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:48:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA16386; Sun, 4 Dec 1994 13:48:33 -0800
Date: Sun, 4 Dec 1994 13:48:33 -0800
From: root (Charlie Root)
Message-Id: <199412042148.NAA16386@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: buf1x3
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: buf1x3
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/********************************************************************/
*                                        *
*       IIIIII  SSSSSS  SSSSSS                   *
*         I    S    S                   *
*         I    S    S                   *
*         I     SSSSS   SSSSS                   *
*         I      S  S                   *
*         I      S  S                   *
*       IIIIII  SSSSSS  SSSSSS                   *
*                                        *
/********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:48:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c buf1x3 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -l -n 16287.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& buf1x3.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2 7/21/94
      lsh: 2.4.15 8/18/94
      vc_engine: 2.4.122 8/30/94
      vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

      vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
      TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: BUF1X3.cmpsum: No such file or directory
grep: BUF1X3.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN BUF1X3.err   **
**   **
****
****

cat buf1x3.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/buf1x3.compare_lpe/buf1x3.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 13:49:38 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id NAA14488; Sun, 4 Dec 1994 13:49:37 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA16503; Sun, 4 Dec 1994 13:49:36 -0800
Date: Sun, 4 Dec 1994 13:49:36 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042149.NAA16503@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 13:49:36 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA16499; Sun, 4 Dec 1994 13:49:36 -0800

Date: Sun, 4 Dec 1994 13:49:36 -0800
From: root (Charlie Root)
Message-Id: <199412042149.NAA16499@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: buf1x4
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: buf1x4
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                 *
*       IIIIIII  SSSSSS  SSSSSS              *
*          I    S     S                *
*          I    S     S                *
*          I     SSSSS   SSSSS              *
*          I        S  S           *
*          I        S  S           *
*       IIIIIII  SSSSSS  SSSSSS              *
*                                 *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:49:04 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c buf1x4 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 16400.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& buf1x4.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2 7/21/94
      lsh: 2.4.15 8/18/94
      vc_engine: 2.4.122 8/30/94
      vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*        Compare summary        *
grep: BUF1X4.cmpsum: No such file or directory
grep: BUF1X4.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                      **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN BUF1X4.err      **
**                      **
*******************************************
*******************************************
```

cat buf1x4.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/buf1x4.compare_lpe/buf1x4.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 13:50:37 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14509; Sun, 4 Dec 1994 13:50:36 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16616; Sun, 4 Dec 1994 13:50:34 -0800
Date: Sun, 4 Dec 1994 13:50:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042150.NAA16616@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job

Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:50:34 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16612; Sun, 4 Dec 1994 13:50:34 -0800
Date: Sun, 4 Dec 1994 13:50:34 -0800
From: root (Charlie Root)
Message-Id: <199412042150.NAA16612@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: c2e
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: c2e
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                  *
*       IIIIII  SSSSSS  SSSSSS            *
*         I    S     S                 *
*         I    S     S                 *
*         I     SSSSS   SSSSS            *
*         I        S     S             *
*         I        S     S             *
*       IIIIII  SSSSSS  SSSSSS            *
*                                  *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:50:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c c2e -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A
datain.dat -h cell.equiv -I -n 16513.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& c2e.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2   7/21/94
        lsh: 2.4.15   8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17   7/11/94
VeriCheck is done.

VeriCheck (R) Hierarchical Design Verification, BETA 2.4.1

Printing individual version numbers ...

    vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
      TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
      TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
      TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
      TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
      TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
      TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
      TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary          *
grep: C2E.cmpsum: No such file or directory
grep: C2E.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                        **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**      PLEASE LOOK IN C2E.err       **
**                        **
*******************************************
*******************************************
```

cat c2e.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/c2e.compare_lpe/c2e.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 13:51:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
      id NAA14530; Sun, 4 Dec 1994 13:51:32 -0800

Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA16731; Sun, 4 Dec 1994 13:51:30 -0800
Date: Sun, 4 Dec 1994 13:51:30 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042151.NAA16731@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:51:30 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA16727; Sun, 4 Dec 1994 13:51:30 -0800
Date: Sun, 4 Dec 1994 13:51:30 -0800
From: root (Charlie Root)
Message-Id: <199412042151.NAA16727@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: def2x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: def2x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/****************************************************************/
*                                *
*       IIIIII   SSSSSS   SSSSSS           *
*          I    S      S              *
*          I    S      S              *
*          I     SSSSS    SSSSS          *
*          I       S      S           *
*          I       S      S           *
*       IIIIII   SSSSSS   SSSSSS           *
*                                *
/****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:51:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c def2x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 16627.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& def2x1.log
Running vericheck
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94

herc: 2.4.2   7/21/94
        lsh: 2.4.15   8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

        vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
        TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
        TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
        TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
        TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
        TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
        TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: DEF2X1.cmpsum: No such file or directory
grep: DEF2X1.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN DEF2X1.err   **
**   **
****
****

cat def2x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/def2x1.compare_lpe/def2x1.lpelog

ISS LPE completed

---------------------- End of Message -------------------------

>From chip Sun Dec 4 13:52:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
     id NAA14551; Sun, 4 Dec 1994 13:52:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id NAA16844; Sun, 4 Dec 1994 13:52:32 -0800
Date: Sun, 4 Dec 1994 13:52:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042152.NAA16844@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -------------------------
>From root Sun Dec 4 13:52:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id NAA16840; Sun, 4 Dec 1994 13:52:31 -0800
Date: Sun, 4 Dec 1994 13:52:31 -0800
From: root (Charlie Root)
Message-Id: <199412042152.NAA16840@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: ef2x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: ef2x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/***********************************************************/
*                                   *
*     IIIIII  SSSSSS  SSSSSS          *
*       I    S    S            *
*       I    S    S            *
*       I    SSSSS   SSSSS          *
*       I      S    S          *
*       I      S    S          *
*     IIIIII  SSSSSS  SSSSSS          *
*                                   *
/***********************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:52:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c ef2x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 16741.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& ef2x1.log
Running vericheck
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94
    herc: 2.4.2   7/21/94
    lsh: 2.4.15   8/18/94
    vc_engine: 2.4.122 8/30/94
    vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*           Compare summary          *
grep: EF2X1.cmpsum: No such file or directory
grep: EF2X1.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                        **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN EF2X1.err      **
```

```
**                    **
*********************************************
*********************************************
```

cat ef2x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/ef2x1.compare_lpe/ef2x1.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 13:53:35 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id NAA14572; Sun, 4 Dec 1994 13:53:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA16958; Sun, 4 Dec 1994 13:53:32 -0800
Date: Sun, 4 Dec 1994 13:53:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042153.NAA16958@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 13:53:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA16954; Sun, 4 Dec 1994 13:53:32 -0800
Date: Sun, 4 Dec 1994 13:53:32 -0800
From: root (Charlie Root)
Message-Id: <199412042153.NAA16954@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: ef3x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: ef3x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/***********************************************************************/
*                                *
*       IIIIII  SSSSSS  SSSSSS           *
*          I   S     S              *
*          I   S     S              *
*          I    SSSSS  SSSSS           *
*          I        S S              *
*          I        S S              *
```

```
*      IIIIIII  SSSSSS  SSSSSS                    *
*                                                 *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:53:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c ef3x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 16855.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& ef3x1.log
Running vericheck
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94
    herc: 2.4.2 7/21/94
    lsh: 2.4.15 8/18/94
    vc_engine: 2.4.122 8/30/94
    vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
********************************************
*          Compare summary          *
grep: EF3X1.cmpsum: No such file or directory
grep: EF3X1.cmpsum: No such file or directory
********************************************
```

```
*******************************************
*******************************************
**                                       **
**   THERE ARE OPENS IN YOUR CIRCUIT  **
**      PLEASE LOOK IN EF3X1.err     **
**                                       **
*******************************************
*******************************************
```

cat ef3x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/ef3x1.compare_lpe/ef3x1.lpelog

ISS LPE completed

----------------------- End of Message ------------------------

>From chip Sun Dec 4 13:54:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
      id NAA14580; Sun, 4 Dec 1994 13:54:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id NAA17071; Sun, 4 Dec 1994 13:54:33 -0800
Date: Sun, 4 Dec 1994 13:54:33 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042154.NAA17071@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message ------------------------
>From root Sun Dec 4 13:54:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id NAA17067; Sun, 4 Dec 1994 13:54:33 -0800
Date: Sun, 4 Dec 1994 13:54:33 -0800
From: root (Charlie Root)
Message-Id: <199412042154.NAA17067@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: eflatch
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: eflatch
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************************/
```

```
*                            *
*    IIIIIII  SSSSSS  SSSSSS          *
*      I    S    S             *
*      I    S    S             *
*      I    SSSSS   SSSSS           *
*      I      S    S            *
*      I      S    S            *
*    IIIIIII  SSSSSS  SSSSSS          *
*                            *
/****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:54:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c eflatch -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 16968.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& eflatch.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2 7/21/94
      lsh: 2.4.15 8/18/94
      vc_engine: 2.4.122 8/30/94
      vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

      vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
      TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
      TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
      TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
      TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
      TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
      TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
      TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: EFLATCH.cmpsum: No such file or directory
grep: EFLATCH.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                        **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN EFLATCH.err       **
**                        **
*******************************************
*******************************************
```

cat eflatch.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/eflatch.compare_lpe/eflatch.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 13:55:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14597; Sun, 4 Dec 1994 13:55:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17184; Sun, 4 Dec 1994 13:55:33 -0800
Date: Sun, 4 Dec 1994 13:55:33 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042155.NAA17184@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 13:55:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17180; Sun, 4 Dec 1994 13:55:33 -0800
Date: Sun, 4 Dec 1994 13:55:33 -0800
From: root (Charlie Root)
Message-Id: <199412042155.NAA17180@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: lat1x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: lat1x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss

```
ISSPATH:         /a/iss
ISS_SYSTYPE:     SUN4
ISS_LSERVER:     hestia
```

user: Undefined variable.

```
/***********************************************************************/
*                                     *
*       IIIIII  SSSSSS   SSSSSS                *
*         I    S      S                   *
*         I    S      S                   *
*         I     SSSSS    SSSSS              *
*         I        S    S                 *
*         I        S    S                 *
*       IIIIII  SSSSSS   SSSSSS                *
*                                     *
/***********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:55:03 PST 1994

```
/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c lat1x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 17081.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& lat1x1.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2  7/21/94
      lsh: 2.4.15  8/18/94
      vc_engine: 2.4.122  8/30/94
      vp: 2.4.17  7/11/94
VeriCheck is done.
```

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Printing individual version numbers ...

      vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
      TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
      TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
      TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
      TEMP layer "n+gateup" defined but never used .

VERICHECK WARNING : At or near line 400:
      TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: LAT1X1.cmpsum: No such file or directory
grep: LAT1X1.cmpsum: No such file or directory
*******************************************



*******************************************
*******************************************
**                         **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**        PLEASE LOOK IN LAT1X1.err      **
**                         **
*******************************************
*******************************************
```

cat lat1x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/lat1x1.compare_lpe/lat1x1.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 13:56:38 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id NAA14618; Sun, 4 Dec 1994 13:56:37 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA17297; Sun, 4 Dec 1994 13:56:34 -0800
Date: Sun, 4 Dec 1994 13:56:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042156.NAA17297@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 13:56:34 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA17293; Sun, 4 Dec 1994 13:56:34 -0800
Date: Sun, 4 Dec 1994 13:56:34 -0800
From: root (Charlie Root)
Message-Id: <199412042156.NAA17293@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: lat1x2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: lat1x2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

```
LTLPATH:       /a/iss
ISSPATH:       /a/iss
ISS_SYSTYPE:   SUN4
ISS_LSERVER:   hestia
```

user: Undefined variable.

```
/*****************************************************************/
*                               *
*      IIIIII  SSSSSS  SSSSSS            *
*        I   S    S              *
*        I   S    S              *
*        I    SSSSS   SSSSS            *
*        I     S    S           *
*        I     S    S           *
*      IIIIII  SSSSSS  SSSSSS            *
*                               *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:56:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c lat1x2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 17194.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& lat1x2.log
Running vericheck
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94
    herc: 2.4.2 7/21/94
    lsh: 2.4.15 8/18/94
    vc_engine: 2.4.122 8/30/94
    vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:

TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
        TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
        TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
        TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
        TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*        Compare summary        *
grep: LAT1X2.cmpsum: No such file or directory
grep: LAT1X2.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                    **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**        PLEASE LOOK IN LAT1X2.err      **
**                    **
*******************************************
*******************************************
```

cat lat1x2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/lat1x2.compare_lpe/lat1x2.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 13:57:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14639; Sun, 4 Dec 1994 13:57:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17410; Sun, 4 Dec 1994 13:57:31 -0800
Date: Sun, 4 Dec 1994 13:57:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042157.NAA17410@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 13:57:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17406; Sun, 4 Dec 1994 13:57:30 -0800
Date: Sun, 4 Dec 1994 13:57:30 -0800
From: root (Charlie Root)
Message-Id: <199412042157.NAA17406@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: lat1x3
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: lat1x3
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                    *
*        IIIIIII  SSSSSS  SSSSSS              *
*           I     S     S                  *
*           I     S     S                  *
*           I      SSSSS   SSSSS              *
*           I          S    S              *
*           I          S    S              *
*        IIIIIII  SSSSSS  SSSSSS              *
*                                    *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:57:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c lat1x3 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 17307.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& lat1x3.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2 7/21/94
      lsh: 2.4.15 8/18/94
      vc_engine: 2.4.122 8/30/94
      vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

      vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*        Compare summary        *
grep: LAT1X3.cmpsum: No such file or directory
grep: LAT1X3.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                       **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN LAT1X3.err      **
**                       **
*******************************************
*******************************************
```

cat lat1x3.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/lat1x3.compare_lpe/lat1x3.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 13:58:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14660; Sun, 4 Dec 1994 13:58:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17523; Sun, 4 Dec 1994 13:58:31 -0800
Date: Sun, 4 Dec 1994 13:58:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042158.NAA17523@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:58:30 1994
Return-Path: <root>

Your "at" job "1989" produced the following output:

Working cell: latch
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: latch
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/******************************************************************/
*                                      *
*       IIIIII  SSSSSS   SSSSSS              *
*         I     S    S                *
*         I     S    S                *
*         I      SSSSS    SSSSS            *
*         I         S    S            *
*         I         S    S            *
*       IIIIII  SSSSSS   SSSSSS              *
*                                      *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:58:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c latch -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 17420.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& latch.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2   7/21/94
        lsh: 2.4.15   8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*        Compare summary          *
grep: LATCH.cmpsum: No such file or directory
grep: LATCH.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                            **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN LATCH.err      **
**                            **
*******************************************
*******************************************
```

cat latch.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/latch.compare_lpe/latch.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 13:59:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id NAA14668; Sun, 4 Dec 1994 13:59:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA17637; Sun, 4 Dec 1994 13:59:31 -0800
Date: Sun, 4 Dec 1994 13:59:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042159.NAA17637@cyclops.microunity.com>

To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:59:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id NAA17633; Sun, 4 Dec 1994 13:59:31 -0800
Date: Sun, 4 Dec 1994 13:59:31 -0800
From: root (Charlie Root)
Message-Id: <199412042159.NAA17633@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: maj
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: maj
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/***************************************************************/
*                               *
*       IIIIII  SSSSSS  SSSSSS             *
*         I    S    S                 *
*         I    S    S                 *
*         I     SSSSS   SSSSS              *
*         I       S   S          *
*         I       S   S          *
*       IIIIII  SSSSSS  SSSSSS             *
*                               *
/***************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:59:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c maj -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 17533.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& maj.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2   7/21/94
      lsh: 2.4.15   8/18/94
      vc_engine: 2.4.122 8/30/94
      vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

        vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
        TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
        TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
        TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
        TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
        TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
        TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: MAJ.cmpsum: No such file or directory
grep: MAJ.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN MAJ.err   **
**   **
****
****

cat maj.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/maj.compare_lpe/maj.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:00:36 1994
Return-Path: <chip>

Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14689; Sun, 4 Dec 1994 14:00:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA17750; Sun, 4 Dec 1994 14:00:34 -0800
Date: Sun, 4 Dec 1994 14:00:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042200.OAA17750@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:00:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA17746; Sun, 4 Dec 1994 14:00:33 -0800
Date: Sun, 4 Dec 1994 14:00:33 -0800
From: root (Charlie Root)
Message-Id: <199412042200.OAA17746@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: mux2x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: mux2x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                       *
*       IIIIII  SSSSSS  SSSSSS               *
*         I   S     S                *
*         I   S     S                *
*         I    SSSSS   SSSSS                   *
*         I      S     S           *
*         I      S     S           *
*       IIIIIII  SSSSSS  SSSSSS               *
*                                       *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:00:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c mux2x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 17647.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& mux2x1.log
Running vericheck

```
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2  7/21/94
        lsh: 2.4.15  8/18/94
        vc_engine: 2.4.122  8/30/94
        vp: 2.4.17  7/11/94
VeriCheck is done.
```

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Printing individual version numbers ...

        vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
        TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
        TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
        TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
        TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
        TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
        TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: MUX2X1.cmpsum: No such file or directory
grep: MUX2X1.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                        **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**        PLEASE LOOK IN MUX2X1.err      **
**                        **
*******************************************
*******************************************
```

cat mux2x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/mux2x1.compare_lpe/mux2x1.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:01:37 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14710; Sun, 4 Dec 1994 14:01:36 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA17865; Sun, 4 Dec 1994 14:01:34 -0800
Date: Sun, 4 Dec 1994 14:01:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042201.OAA17865@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:01:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA17861; Sun, 4 Dec 1994 14:01:33 -0800
Date: Sun, 4 Dec 1994 14:01:33 -0800
From: root (Charlie Root)
Message-Id: <199412042201.OAA17861@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: mux2x2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: mux2x2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/******************************************************************/
*                                    *
*        IIIIIII  SSSSSS  SSSSSS           *
*           I   S      S              *
*           I   S      S              *
*           I    SSSSS   SSSSS              *
*           I      S      S           *
*           I      S      S           *
*        IIIIIII  SSSSSS  SSSSSS           *
*                                    *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:01:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c mux2x2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 17762.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& mux2x2.log
Running vericheck
     gdsin: 5.1.2 6/22/94
     gdsout: 5.1.8 6/6/94
     herc: 2.4.2 7/21/94
     lsh: 2.4.15 8/18/94
     vc_engine: 2.4.122 8/30/94
     vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

     vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
     TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
     TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
     TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
     TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
     TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
     TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
     TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: MUX2X2.cmpsum: No such file or directory
grep: MUX2X2.cmpsum: No such file or directory
****

****
****
**   **

```
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN MUX2X2.err      **
**                                      **
******************************************
******************************************
```

cat mux2x2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/mux2x2.compare_lpe/mux2x2.lpelog

ISS LPE completed

----------------------- End of Message --------------------------

>From chip Sun Dec 4 14:02:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
     id OAA14731; Sun, 4 Dec 1994 14:02:36 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id OAA17978; Sun, 4 Dec 1994 14:02:34 -0800
Date: Sun, 4 Dec 1994 14:02:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042202.OAA17978@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message ----------------------
>From root Sun Dec 4 14:02:34 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id OAA17974; Sun, 4 Dec 1994 14:02:34 -0800
Date: Sun, 4 Dec 1994 14:02:34 -0800
From: root (Charlie Root)
Message-Id: <199412042202.OAA17974@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: mux3x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: mux3x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                              *
*       IIIIII  SSSSSS  SSSSSS            *
*         I    S     S                *
*         I    S     S                *
*         I     SSSSS  SSSSS             *
```

```
*        I      S       S                *
*        I      S       S                *
*      IIIIIII  SSSSSS   SSSSSS             *
*                                *
/*********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:02:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c mux3x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 17875.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& mux3x1.log
Running vericheck
     gdsin: 5.1.2 6/22/94
     gdsout: 5.1.8 6/6/94
     herc: 2.4.2   7/21/94
     lsh: 2.4.15   8/18/94
     vc_engine: 2.4.122 8/30/94
     vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

     vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
     TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
     TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
     TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
     TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
     TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
     TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
     TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*****************************************
*         Compare summary          *
```
grep: MUX3X1.cmpsum: No such file or directory

grep: MUX3X1.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN MUX3X1.err   **
**   **
****
****

cat mux3x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/mux3x1.compare_lpe/mux3x1.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:03:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
       id OAA14752; Sun, 4 Dec 1994 14:03:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
       id OAA18091; Sun, 4 Dec 1994 14:03:32 -0800
Date: Sun, 4 Dec 1994 14:03:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042203.OAA18091@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:03:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
       id OAA18087; Sun, 4 Dec 1994 14:03:31 -0800
Date: Sun, 4 Dec 1994 14:03:31 -0800
From: root (Charlie Root)
Message-Id: <199412042203.OAA18087@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: mux3x2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: mux3x2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                      *
*      IIIIII  SSSSSS  SSSSSS              *
*        I    S      S               *
*        I    S      S               *
*        I     SSSSS   SSSSS             *
*        I        S    S          *
*        I        S    S          *
*      IIIIII  SSSSSS  SSSSSS              *
*                                      *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:03:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c mux3x2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 17988.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& mux3x2.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

        vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
        TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
        TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
        TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
        TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
        TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:

TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: MUX3X2.cmpsum: No such file or directory
grep: MUX3X2.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                          **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**       PLEASE LOOK IN MUX3X2.err      **
**                          **
*******************************************
*******************************************
```

cat mux3x2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/mux3x2.compare_lpe/mux3x2.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:04:35 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14764; Sun, 4 Dec 1994 14:04:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18204; Sun, 4 Dec 1994 14:04:32 -0800
Date: Sun, 4 Dec 1994 14:04:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042204.OAA18204@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:04:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18200; Sun, 4 Dec 1994 14:04:32 -0800
Date: Sun, 4 Dec 1994 14:04:32 -0800
From: root (Charlie Root)
Message-Id: <199412042204.OAA18200@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or10
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or10
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

```
LTLPATH:        /a/iss
ISSPATH:        /a/iss
ISS_SYSTYPE:    SUN4
ISS_LSERVER:    hestia
```

user: Undefined variable.

```
/*******************************************************************/
*                                       *
*       IIIIII  SSSSSS  SSSSSS                  *
*         I    S    S                *
*         I    S    S                *
*         I     SSSSS   SSSSS                 *
*         I      S  S                *
*         I      S  S                *
*       IIIIII  SSSSSS  SSSSSS                  *
*                                       *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:04:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or10 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 18101.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or10.log
Running vericheck
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94
    herc: 2.4.2 7/21/94
    lsh: 2.4.15 8/18/94
    vc_engine: 2.4.122 8/30/94
    vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

```

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
****
*   Compare summary   *
grep: OR10.cmpsum: No such file or directory
grep: OR10.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN OR10.err   **
**   **
****
****
```

cat or10.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or10.compare_lpe/or10.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec  4 14:05:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14777; Sun, 4 Dec 1994 14:05:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18317; Sun, 4 Dec 1994 14:05:32 -0800
Date: Sun, 4 Dec 1994 14:05:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042205.OAA18317@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root  Sun Dec  4 14:05:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18313; Sun, 4 Dec 1994 14:05:32 -0800
Date: Sun, 4 Dec 1994 14:05:32 -0800
From: root (Charlie Root)
Message-Id: <199412042205.OAA18313@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:


Working cell: or11

Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or11
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH:        /a/iss
ISSPATH:        /a/iss
ISS_SYSTYPE:    SUN4
ISS_LSERVER:    hestia

user: Undefined variable.

```
/**********************************************************************/
*                                    *
*       IIIIII  SSSSSS  SSSSSS            *
*         I    S     S              *
*         I    S     S              *
*         I     SSSSS    SSSSS             *
*         I       S   S          *
*         I       S   S          *
*       IIIIII  SSSSSS   SSSSSS            *
*                                    *
/**********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:05:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or11 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 18214.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or11.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2 7/21/94
      lsh: 2.4.15 8/18/94
      vc_engine: 2.4.122 8/30/94
      vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

      vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
      TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
      TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary         *
grep: OR11.cmpsum: No such file or directory
grep: OR11.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                             **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**        PLEASE LOOK IN OR11.err        **
**                             **
*******************************************
*******************************************
```

cat or11.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or11.compare_lpe/or11.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:06:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14798; Sun, 4 Dec 1994 14:06:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18430; Sun, 4 Dec 1994 14:06:32 -0800
Date: Sun, 4 Dec 1994 14:06:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042206.OAA18430@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:06:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18426; Sun, 4 Dec 1994 14:06:32 -0800
Date: Sun, 4 Dec 1994 14:06:32 -0800
From: root (Charlie Root)
Message-Id: <199412042206.OAA18426@cyclops.microunity.com>

To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or12
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or12
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                        *
*       IIIIIII  SSSSSS   SSSSSS              *
*          I    S     S                  *
*          I    S     S                  *
*          I     SSSSS    SSSSS              *
*          I        S   S                 *
*          I        S   S                 *
*       IIIIII   SSSSSS   SSSSSS              *
*                                        *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:06:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or12 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 18327.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or12.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
     TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
     TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
     TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
     TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
     TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
     TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
     TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary          *
grep: OR12.cmpsum: No such file or directory
grep: OR12.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                            **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**       PLEASE LOOK IN OR12.err      **
**                            **
*******************************************
*******************************************
```

cat or12.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or12.compare_lpe/or12.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:08:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
     id OAA14836; Sun, 4 Dec 1994 14:08:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id OAA18544; Sun, 4 Dec 1994 14:08:34 -0800
Date: Sun, 4 Dec 1994 14:08:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042208.OAA18544@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------

>From root Sun Dec 4 14:08:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18540; Sun, 4 Dec 1994 14:08:33 -0800
Date: Sun, 4 Dec 1994 14:08:33 -0800
From: root (Charlie Root)
Message-Id: <199412042208.OAA18540@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or13
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or13
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                       *
*       IIIIII   SSSSSS   SSSSSS                 *
*         I    S      S                      *
*         I    S      S                      *
*         I      SSSSS    SSSSS                    *
*         I        S    S                    *
*         I        S    S                    *
*       IIIIII   SSSSSS   SSSSSS                 *
*                                       *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:08:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or13 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 18441.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or13.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: OR13.cmpsum: No such file or directory
grep: OR13.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                              **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**        PLEASE LOOK IN OR13.err      **
**                              **
*******************************************
*******************************************
```

cat or13.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or13.compare_lpe/or13.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:09:35 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14857; Sun, 4 Dec 1994 14:09:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18658; Sun, 4 Dec 1994 14:09:33 -0800
Date: Sun, 4 Dec 1994 14:09:33 -0800

From: chip (Buffalo Chip)
Message-Id: <199412042209.OAA18658@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:09:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18654; Sun, 4 Dec 1994 14:09:32 -0800
Date: Sun, 4 Dec 1994 14:09:32 -0800
From: root (Charlie Root)
Message-Id: <199412042209.OAA18654@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or14
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or14
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/************************************************************/
*                                    *
*      IIIIII   SSSSSS   SSSSSS           *
*         I    S      S                *
*         I    S      S                *
*         I      SSSSS    SSSSS            *
*         I        S      S            *
*         I        S      S            *
*      IIIIII   SSSSSS   SSSSSS            *
*                                    *
/************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:09:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or14 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 18555.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or14.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2 7/21/94
      lsh: 2.4.15 8/18/94
      vc_engine: 2.4.122 8/30/94

vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: OR14.cmpsum: No such file or directory
grep: OR14.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN OR14.err   **
**   **
****
****

cat or14.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or14.compare_lpe/or14.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:10:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14865; Sun, 4 Dec 1994 14:10:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18771; Sun, 4 Dec 1994 14:10:32 -0800
Date: Sun, 4 Dec 1994 14:10:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042210.OAA18771@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:10:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18767; Sun, 4 Dec 1994 14:10:31 -0800
Date: Sun, 4 Dec 1994 14:10:31 -0800
From: root (Charlie Root)
Message-Id: <199412042210.OAA18767@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or15
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or15
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

/**/
*   *
*   IIIIII SSSSSS SSSSSS   *
*   I   S   S   *
*   I   S   S   *
*   I   SSSSS   SSSSS   *
*   I   S S   *
*   I   S S   *
*   IIIIII SSSSSS SSSSSS   *
*   *
/**/

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:10:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or15 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 18668.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-

cp/tools/lib/stream/mobimos1.tbl >>& or15.log
Running vericheck
     gdsin: 5.1.2 6/22/94
     gdsout: 5.1.8 6/6/94
     herc: 2.4.2 7/21/94
     lsh: 2.4.15 8/18/94
     vc_engine: 2.4.122 8/30/94
     vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

     vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
     TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
     TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
     TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
     TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
     TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
     TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
     TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary         *
grep: OR15.cmpsum: No such file or directory
grep: OR15.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                    **
**     THERE ARE OPENS IN YOUR CIRCUIT    **
**        PLEASE LOOK IN OR15.err     **
**                    **
*******************************************
*******************************************
```

cat or15.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or15.compare_lpe/or15.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:11:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14882; Sun, 4 Dec 1994 14:11:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18885; Sun, 4 Dec 1994 14:11:31 -0800
Date: Sun, 4 Dec 1994 14:11:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042211.OAA18885@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:11:30 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18881; Sun, 4 Dec 1994 14:11:30 -0800
Date: Sun, 4 Dec 1994 14:11:30 -0800
From: root (Charlie Root)
Message-Id: <199412042211.OAA18881@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or16
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or16
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                   *
*       IIIIII   SSSSSS   SSSSSS          *
*         I    S      S            *
*         I    S      S            *
*         I     SSSSS   SSSSS            *
*         I      S      S          *
*         I      S      S          *
*       IIIIII   SSSSSS   SSSSSS          *
*                                   *
/*****************************************************************/
```

cat or15.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or15.compare_lpe/or15.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:11:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14882; Sun, 4 Dec 1994 14:11:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18885; Sun, 4 Dec 1994 14:11:31 -0800
Date: Sun, 4 Dec 1994 14:11:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042211.OAA18885@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:11:30 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18881; Sun, 4 Dec 1994 14:11:30 -0800
Date: Sun, 4 Dec 1994 14:11:30 -0800
From: root (Charlie Root)
Message-Id: <199412042211.OAA18881@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or16
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or16
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                   *
*       IIIIII   SSSSSS   SSSSSS          *
*         I    S      S            *
*         I    S      S            *
*         I     SSSSS   SSSSS            *
*         I      S      S          *
*         I      S      S          *
*       IIIIII   SSSSSS   SSSSSS          *
*                                   *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:11:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or16 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 18782.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or16.log
Running vericheck
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94
    herc: 2.4.2 7/21/94
    lsh: 2.4.15 8/18/94
    vc_engine: 2.4.122 8/30/94
    vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: OR16.cmpsum: No such file or directory
grep: OR16.cmpsum: No such file or directory
****

****

```
************************************************
**                                          **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN OR16.err        **
**                                          **
************************************************
************************************************
```

cat or16.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or16.compare_lpe/or16.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:12:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
     id OAA14903; Sun, 4 Dec 1994 14:12:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id OAA18998; Sun, 4 Dec 1994 14:12:30 -0800
Date: Sun, 4 Dec 1994 14:12:30 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042212.OAA18998@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:12:30 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id OAA18994; Sun, 4 Dec 1994 14:12:30 -0800
Date: Sun, 4 Dec 1994 14:12:30 -0800
From: root (Charlie Root)
Message-Id: <199412042212.OAA18994@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or17
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or17
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/**********************************************************************/
*                                      *
*                                                    *
*       IIIIII   SSSSSS   SSSSSS                 *
*          I     S        S                    *
```

```
*       I   S    S               *
*       I  SSSSS  SSSSS              *
*       I    S   S             *
*       I    S   S             *
*      IIIIII SSSSSS  SSSSSS          *
*                         *
/****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:12:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or17 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 18895.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or17.log
Running vericheck
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94
    herc: 2.4.2   7/21/94
    lsh: 2.4.15   8/18/94
    vc_engine: 2.4.122 8/30/94
    vp: 2.4.17   7/11/94
VeriCheck is done.

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    vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****

```
*         Compare summary        *
grep: OR17.cmpsum: No such file or directory
grep: OR17.cmpsum: No such file or directory
********************************************


********************************************
********************************************
**                           **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN OR17.err       **
**                           **
********************************************
********************************************
```

cat or17.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or17.compare_lpe/or17.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:13:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
     id OAA14924; Sun, 4 Dec 1994 14:13:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id OAA19111; Sun, 4 Dec 1994 14:13:31 -0800
Date: Sun, 4 Dec 1994 14:13:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042213.OAA19111@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:13:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id OAA19107; Sun, 4 Dec 1994 14:13:31 -0800
Date: Sun, 4 Dec 1994 14:13:31 -0800
From: root (Charlie Root)
Message-Id: <199412042213.OAA19107@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/****************************************************************/
*                                    *
*        IIIIIII  SSSSSS   SSSSSS          *
*           I    S     S        *
*           I    S     S        *
*           I     SSSSS    SSSSS        *
*           I       S    S      *
*           I       S    S      *
*        IIIIIII  SSSSSS   SSSSSS          *
*                                    *
/****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:13:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 19008.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& or2.log
Running vericheck
     gdsin: 5.1.2 6/22/94
     gdsout: 5.1.8 6/6/94
     herc: 2.4.2 7/21/94
     lsh: 2.4.15 8/18/94
     vc_engine: 2.4.122 8/30/94
     vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

     vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
     TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
     TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
     TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
     TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
     TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
     TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
********************************************
*         Compare summary         *
grep: OR2.cmpsum: No such file or directory
grep: OR2.cmpsum: No such file or directory
********************************************


********************************************
********************************************
**                              **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**       PLEASE LOOK IN OR2.err       **
**                              **
********************************************
********************************************
```

cat or2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or2.compare_lpe/or2.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:14:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14945; Sun, 4 Dec 1994 14:14:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA19224; Sun, 4 Dec 1994 14:14:32 -0800
Date: Sun, 4 Dec 1994 14:14:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042214.OAA19224@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:14:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA19220; Sun, 4 Dec 1994 14:14:31 -0800
Date: Sun, 4 Dec 1994 14:14:31 -0800
From: root (Charlie Root)
Message-Id: <199412042214.OAA19220@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or3
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or3

rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*************************************************************/
*                                    *
*      IIIIII  SSSSSS  SSSSSS            *
*       I    S    S                *
*       I    S    S                *
*       I    SSSSS  SSSSS            *
*       I     S    S               *
*       I     S    S               *
*      IIIIII SSSSSS  SSSSSS            *
*                                    *
/*************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:14:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or3 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A
datain.dat -h cell.equiv -I -n 19121.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or3.log
Running vericheck
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94
    herc: 2.4.2   7/21/94
    lsh: 2.4.15   8/18/94
    vc_engine: 2.4.122 8/30/94
    vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:

TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*****************************************
*         Compare summary        *
grep: OR3.cmpsum: No such file or directory
grep: OR3.cmpsum: No such file or directory
*****************************************


*****************************************
*****************************************
**                       **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN OR3.err      **
**                       **
*****************************************
*****************************************
```

cat or3.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or3.compare_lpe/or3.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:15:35 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14961; Sun, 4 Dec 1994 14:15:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA19338; Sun, 4 Dec 1994 14:15:32 -0800
Date: Sun, 4 Dec 1994 14:15:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042215.OAA19338@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:15:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA19334; Sun, 4 Dec 1994 14:15:32 -0800
Date: Sun, 4 Dec 1994 14:15:32 -0800
From: root (Charlie Root)
Message-Id: <199412042215.OAA19334@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or4
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or4
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/***********************************************************************/
*                                 *
*      IIIIII  SSSSSS  SSSSSS             *
*       I    S    S                *
*       I    S    S                *
*       I    SSSSS   SSSSS             *
*       I      S    S            *
*       I      S    S            *
*      IIIIII  SSSSSS  SSSSSS             *
*                                 *
/***********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:15:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or4 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A
datain.dat -h cell.equiv -I -n 19234.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or4.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2 7/21/94
      lsh: 2.4.15 8/18/94
      vc_engine: 2.4.122 8/30/94
      vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

      vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
      TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: OR4.cmpsum: No such file or directory
grep: OR4.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN OR4.err   **
**   **
****
****

cat or4.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or4.compare_lpe/or4.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:16:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14974; Sun, 4 Dec 1994 14:16:36 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19451; Sun, 4 Dec 1994 14:16:34 -0800
Date: Sun, 4 Dec 1994 14:16:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042216.OAA19451@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:16:34 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19447; Sun, 4 Dec 1994 14:16:34 -0800
Date: Sun, 4 Dec 1994 14:16:34 -0800

From: root (Charlie Root)
Message-Id: <199412042216.OAA19447@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or5
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or5
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                               *                *
*       IIIIII  SSSSSS  SSSSSS          *
*         I    S     S                *
*         I    S     S                *
*         I     SSSSS   SSSSS            *
*         I        S     S            *
*         I        S     S            *
*       IIIIII  SSSSSS   SSSSSS          *
*                               *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:16:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or5 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A
datain.dat -h cell.equiv -I -n 19348.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or5.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
******************************************
*         Compare summary         *
grep: OR5.cmpsum: No such file or directory
grep: OR5.cmpsum: No such file or directory
******************************************


******************************************
******************************************
**                       **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN OR5.err      **
**                       **
******************************************
******************************************
```

cat or5.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or5.compare_lpe/or5.lpelog

ISS LPE completed

------------------------- End of Message -------------------------

>From chip Sun Dec 4 14:17:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14995; Sun, 4 Dec 1994 14:17:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA19565; Sun, 4 Dec 1994 14:17:32 -0800
Date: Sun, 4 Dec 1994 14:17:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042217.OAA19565@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

>From root Sun Dec 4 14:17:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19561; Sun, 4 Dec 1994 14:17:32 -0800
Date: Sun, 4 Dec 1994 14:17:32 -0800
From: root (Charlie Root)
Message-Id: <199412042217.OAA19561@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or6
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or6
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                         *
*      IIIIII  SSSSSS   SSSSSS                *
*        I    S     S                   *
*        I    S     S                   *
*        I     SSSSS    SSSSS                 *
*        I        S    S               *
*        I        S    S               *
*      IIIIII  SSSSSS   SSSSSS                *
*                                         *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:17:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or6 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A
datain.dat -h cell.equiv -I -n 19462.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or6.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2   7/21/94
        lsh: 2.4.15   8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*********************************************
*          Compare summary          *
grep: OR6.cmpsum: No such file or directory
grep: OR6.cmpsum: No such file or directory
*********************************************


*********************************************
*********************************************
**                          **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**        PLEASE LOOK IN OR6.err       **
**                          **
*********************************************
*********************************************
```

cat or6.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or6.compare_lpe/or6.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:18:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA15016; Sun, 4 Dec 1994 14:18:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)

id OAA19678; Sun, 4 Dec 1994 14:18:32 -0800
Date: Sun, 4 Dec 1994 14:18:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042218.OAA19678@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:18:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19674; Sun, 4 Dec 1994 14:18:31 -0800
Date: Sun, 4 Dec 1994 14:18:31 -0800
From: root (Charlie Root)
Message-Id: <199412042218.OAA19674@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or7
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or7
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/***********************************************************************/
*                                    *
*       IIIIII  SSSSSS  SSSSSS               *
*         I    S     S                    *
*         I    S     S                    *
*         I     SSSSS   SSSSS              *
*         I        S  S                   *
*         I        S  S                   *
*       IIIIII  SSSSSS  SSSSSS               *
*                                    *
/***********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:18:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or7 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A
datain.dat -h cell.equiv -I -n 19575.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or7.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2 7/21/94

lsh: 2.4.15 8/18/94
vc_engine: 2.4.122 8/30/94
vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*********************************************
*         Compare summary         *
grep: OR7.cmpsum: No such file or directory
grep: OR7.cmpsum: No such file or directory
*********************************************


*********************************************
*********************************************
**                     **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN OR7.err      **
**                     **
*********************************************
*********************************************
```

cat or7.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or7.compare_lpe/or7.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:20:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA15054; Sun, 4 Dec 1994 14:20:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19791; Sun, 4 Dec 1994 14:20:34 -0800
Date: Sun, 4 Dec 1994 14:20:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042220.OAA19791@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:20:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19787; Sun, 4 Dec 1994 14:20:33 -0800
Date: Sun, 4 Dec 1994 14:20:33 -0800
From: root (Charlie Root)
Message-Id: <199412042220.OAA19787@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or8
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or8
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/******************************************************************/
*                                        *
*       IIIIII  SSSSSS  SSSSSS               *
*         I    S     S                  *
*         I    S     S                  *
*         I     SSSSS   SSSSS                *
*         I        S    S               *
*         I        S    S               *
*       IIIIII  SSSSSS  SSSSSS               *
*                                        *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:20:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or8 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A
datain.dat -h cell.equiv -I -n 19688.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or8.log
Running vericheck
      gdsin: 5.1.2 6/22/94
      gdsout: 5.1.8 6/6/94
      herc: 2.4.2 7/21/94
      lsh: 2.4.15 8/18/94
      vc_engine: 2.4.122 8/30/94
      vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

      vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
      TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
      TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
      TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
      TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
      TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
      TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
      TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: OR8.cmpsum: No such file or directory
grep: OR8.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN OR8.err   **
**   **

```
*********************************************
*********************************************

cat or8.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or8.compare_lpe/or8.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec  4 14:22:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA15075; Sun, 4 Dec 1994 14:22:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19905; Sun, 4 Dec 1994 14:22:34 -0800
Date: Sun, 4 Dec 1994 14:22:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042222.OAA19905@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O


----------------------- Start of Message -----------------------
>From root  Sun Dec  4 14:22:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19901; Sun, 4 Dec 1994 14:22:33 -0800
Date: Sun, 4 Dec 1994 14:22:33 -0800
From: root (Charlie Root)
Message-Id: <199412042222.OAA19901@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:


Working cell: or9
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl


Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or9
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH:        /a/iss
ISSPATH:        /a/iss
ISS_SYSTYPE:    SUN4
ISS_LSERVER:    hestia

user: Undefined variable.

/*************************************************************************/
*                                    *
*       IIIIII  SSSSSS  SSSSSS             *
*         I    S      S                *
*         I    S      S                *
*         I     SSSSS   SSSSS                *
*         I         S      S           *
*         I         S      S           *
*       IIIIII  SSSSSS  SSSSSS              *
```

```
 *                              *
/****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:22:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or9 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A
datain.dat -h cell.equiv -I -n 19802.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or9.log
Running vericheck
 gdsin: 5.1.2 6/22/94
 gdsout: 5.1.8 6/6/94
 herc: 2.4.2   7/21/94
 lsh: 2.4.15   8/18/94
 vc_engine: 2.4.122 8/30/94
 vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

 vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
 TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
 TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
 TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
 TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
 TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
 TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
 TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
********************************************
*          Compare summary          *
```
grep: OR9.cmpsum: No such file or directory
grep: OR9.cmpsum: No such file or directory
```
********************************************
```

```
**********************************************
**********************************************
**                        **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN OR9.err      **
**                        **
**********************************************
**********************************************
```

cat or9.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or9.compare_lpe/or9.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:24:40 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA15113; Sun, 4 Dec 1994 14:24:39 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA20019; Sun, 4 Dec 1994 14:24:34 -0800
Date: Sun, 4 Dec 1994 14:24:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042224.OAA20019@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:24:34 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA20015; Sun, 4 Dec 1994 14:24:34 -0800
Date: Sun, 4 Dec 1994 14:24:34 -0800
From: root (Charlie Root)
Message-Id: <199412042224.OAA20015@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: switch2px1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: switch2px1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/************************************************************************/
*                                    *
```

```
*      IIIIII  SSSSSS  SSSSSS                    *
*        I    S      S                  *
*        I    S      S                  *
*        I     SSSSS   SSSSS                 *
*        I        S      S             *
*        I        S      S             *
*      IIIIII  SSSSSS  SSSSSS               *
*                                        *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:24:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c switch2px1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 19916.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& switch2px1.log
Running vericheck
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94
    herc: 2.4.2   7/21/94
    lsh: 2.4.15   8/18/94
    vc_engine: 2.4.122 8/30/94
    vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*********************************************
*        Compare summary         *
grep: SWITCH2PX1.cmpsum: No such file or directory
grep: SWITCH2PX1.cmpsum: No such file or directory
*********************************************


*********************************************
*********************************************
**                        **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN SWITCH2PX1.err      **
**                        **
*********************************************
*********************************************


cat switch2px1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/switch2px1.compare_lpe/switch2px1.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec  4 14:25:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA15134; Sun, 4 Dec 1994 14:25:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA20133; Sun, 4 Dec 1994 14:25:34 -0800
Date: Sun, 4 Dec 1994 14:25:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042225.OAA20133@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root  Sun Dec  4 14:25:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA20129; Sun, 4 Dec 1994 14:25:33 -0800
Date: Sun, 4 Dec 1994 14:25:33 -0800
From: root (Charlie Root)
Message-Id: <199412042225.OAA20129@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:


Working cell: switch2px2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: switch2px2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH:        /a/iss
ISSPATH:        /a/iss
```

```
ISS_SYSTYPE:    SUN4
ISS_LSERVER:    hestia

user: Undefined variable.

/*********************************************************************/
*                                          *
*      IIIIII   SSSSSS   SSSSSS                *
*         I    S        S                  *
*         I    S        S                  *
*         I      SSSSS   SSSSS                *
*         I          S        S            *
*         I          S        S            *
*      IIIIII   SSSSSS   SSSSSS                *
*                                          *
/*********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:25:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c switch2px2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 20030.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& switch2px2.log
Running vericheck
     gdsin: 5.1.2 6/22/94
     gdsout: 5.1.8 6/6/94
     herc: 2.4.2   7/21/94
     lsh: 2.4.15   8/18/94
     vc_engine: 2.4.122 8/30/94
     vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

     vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
     TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
     TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
     TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
     TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
     TEMP layer "gatepoly" defined but never used

Exhibit C9   Page 130 of 564
```

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*********************************************
*         Compare summary          *
grep: SWITCH2PX2.cmpsum: No such file or directory
grep: SWITCH2PX2.cmpsum: No such file or directory
*********************************************


*********************************************
*********************************************
**                      **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN SWITCH2PX2.err     **
**                      **
*********************************************
*********************************************
```

cat switch2px2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/switch2px2.compare_lpe/switch2px2.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

From:	geert (Geert Rosseel)
Sent:	Monday, December 05, 1994 12:09 PM
To:	'billz'; 'brianl'; 'dickson'; 'geert'; 'hopper'; 'mws'; 'tbr'; 'vo'; 'woody'
Subject:	Euterpe status

Hi,

Over the weekend, I built a top-level version of euterpe in the snapshot. I have
currently a route going in the snapshot. I also did a route locally and it finished up to
99.2 % (about 1500 missing connections).

What I'd like to do after this is get the newest BOM in the snapshot
(188.0) and rebuild all subblocks that need to be. There is a problem in the snapshot
because of some inconsistency. I should be able to get that done by tomorrow morning.

New list of things to do follows. As usual, if you release a BOM in /u/chip, please
page me (releasebom -P geert)

The goal is to get all this done by **** Tuesday Evening ***.

If we get this, we should be able to assemble the left half of the control strip on
Wednesday. During the second half of this week, we can work on the remaining part.


```
iq, cp, cj, ctioi : placements of all 4 blocks
                    fix obstruction mask problem

   -- cj looks really big. It used to be a lot smaller.

       Brianl

cc  : place
          x0 = 1629
          y0 = 404
          height < 82 rows

   -- A new BOM was released after the latest placement. Can you
      check if placement is still O.K.

      Rich

hc  : place
        Jay

at  : place
          x0 = 480
          y0 = 404
          height up to dcache
          width up to spar at left of GTLB
        Jay

nb :  placement outline is O.K., however, internals have to be changed.
      Datapath section in non-ea part should be aligned with exlax array.
      Control should live on the right and UNDER the datapath section (rather
      than above). nb should not extend beyond clock-spar at the right edge.

      Hopper

dr : align right edge
```

```
          check for fan-out problems ( < 50ps margin paths)
             Billz

icc : place
          x0 = 2938
          1 spar-section wide.
          place under the iq, cj, cp, section such that
          the top of icc aligns with the bottom of the
          TBL, Icache

    -- New BOM was released, no placement in /u/chip

       Hopper

ife : size estimate
       Rich

uu   : size estimate
       Mark (S.)

lt   : shift long narrow part to the right by 16 atoms.
       shorten the long row in the lower part of lt.
       Jay

hz   : place
          x0 = 2938
          y0 = 527
          one spar-section wide
        Rich
```

From: brianl (Brian Lee)
Sent: Monday, December 05, 1994 12:40 PM
To: 'Geert Rosseel'
Subject: Re: Euterpe status

Geert Rosseel writes:

> iq, cp, cj, ctioi : placements of all 4 blocks
>   fix obstruction mask problem

Hmmm. I thought I fixed this. Is this still a problem? Is there a way for me to view your top level results?

> -- cj looks really big. It used to be a lot smaller.
>
>   Brianl

We did add buffers to the snake bus so that it could be multicycle. We also added directives to the power.tab.local so that topt wouldn't time the bus. Sounds like these buffers are getting sized at the top level when the intent was for them not to grow ... unless they need to be larger for dc load considerations.

--
    Brian L.

From:	woody (Jay Tomlinson)
Sent:	Monday, December 05, 1994 1:01 PM
To:	'geert (Geert Rosseel)'
Cc:	'billz'; 'brianl'; 'dickson'; 'geert'; 'hopper'; 'mws'; 'tbr'; 'vo'
Subject:	Euterpe status

Geert Rosseel wrote (on Mon Dec 5):

```
    at   : place
             x0 = 480
             y0 = 404
             height up to dcache
             width up to spar at left of GTLB
         Jay
```

Are you sure about this yoffset? This puts at below the mast.
Jay

From: pmayer (Patricia Mayer)
Sent: Monday, December 05, 1994 1:01 PM
To: 'hestia'; 'tbe@MicroUnity.com'
Cc: 'glen'
Subject: new Main PWB gerbers

My apologies. I left the design review Thursday and did edits as I understood them. All
edits now done according to the following memo.
New plots available.

> From tbe@MicroUnity.com Thu Dec 1 13:17:08 1994
> Date: Thu, 1 Dec 94 13:17:02 PST
> X-Sender: tbe@gaea.microunity.com
> Mime-Version: 1.0
> Content-Type> : > text/plain> ; > charset="us-ascii">
> To: hestia
> From: tbe@MicroUnity.com
> Subject: minutes from final pcb review of 12/1
> Cc: glen
> Content-Length: 3841
>
> Following are results from the review; the first four items must be
> completed before the pcb is released to fab, the other actions do not
> impact the fab.
>
> 1) The "A" reference designator silkscreen on top and bottom will be
mostly
> obliterated by the rout line.
>
> Action: Pattie to remove this character from both silkscreens.
DONE
>
> 2) The pcb should be released at revision 1; current marking says
revision A.
>
> Action: Pattie to correct revision marking at all locations.
DONE
>
> 3) There needs to be a clearance in the soldermask for Calliope and
Euterpe
> ground return under their space transformers. The via field in that
ground
> pad requires that the bottom soldermask also have clearances.
>
> Action: Pattie to add same size clearances for the Ca/Eu ground pads
> on both top and bottom soldermasks.
DONE

From: geert (Geert Rosseel)

Sent: Monday, December 05, 1994 1:49 PM

To: 'wampler'

Cc: 'hopper'; 'tbr'; 'vo'

Subject: Euterpe Route

Hi Kurt,

I would like to ask you to take responsibility for the Euterpe
route for a while. I am too caught up in the placement to make any
reasonable progress on the route.

I woeked over the weekend on getting the euterpe snapshot in good
sahpe so there is a good databse you can work from. There is
currently a route running in the snapshot. It will be done later this
afternoon.

The snapshot gards directory will not change for a while. This is
writable by anybody. You can also change the Makefiles in bsrc
as long as you check them in immediately si that they get
included in the next BOM.

The snapshot is in :

/n/auspex/s41/euterpe-snapshot/euterpe/verilog/bsrc

      Thank's

      Geert

From:	tbr (Tim B. Robinson)
Sent:	Monday, December 05, 1994 2:10 PM
To:	'bobm'; 'dickson'; 'woody'; 'billx'; 'mws'; 'jeffm'
Cc:	'euterpe'
Subject:	I buffer page size

Here's the history, it looks like this did not get propagated to the uarch doc. Bob please amend.

We allocated bits 59:55 in octlet 6, to encode n for a pagesize of 2^n bytes (analagous to icache and dcache page sizes. n is >= 6.
Lets make the default 6 (the default was never discussed).

```
------- Start of forwarded message -------
Status: RO
X-VM-v5-Data: ([nil nil nil nil nil nil nil nil nil]
        ["1358" "Mon" "24" "October" "94" "08:17:23" "PDT" "tbr" "tbr"
nil "37" "forwarded message from tbr" "^To:" nil nil "10"])
To: craig
cc: mws
Subject: forwarded message from tbr
```

Craig, mark is now stuck for this. If I understand what we need correctly, we need to be able to specify a power of 2 boundary, the crossing of which would cause ifetch to stumble to steal a GTLB cycle.

If we encode this the same we as we ancode the cache configuration fields (ie storning the n in 2^n) then a 5 bit field with a minimum value of 6 would seem to be all we need. We micht just be able to squeeze that into octlet 6. We currently have 7 spare bits in 59:53 (though we need some reserved for possible expansion of NB priority).

So, if this is acceptable to you, I propose we decode bits 59:55.

Tim

```
- ------- Start of forwarded message -------
To: craig
cc: euterpe
Subject: I buffer proection
```

Here's another one we need an answer for please:

In article <199404080456.VAA01042@aphrodite.microunity.com>, tbr@aphrodite.microunity.com (Tim B. Robinson) writes:
```
>
> There is a problem with protection of the IB now we have doubled the
> throughput of the Dcache since the I side no longer has access to the GTLB.
> Craig proposes an architecturally defined register to set the protection
> granularity. Crossing a protection boundary or taking a branch causes the
> I side to steal a cycle from the GTLB and cache the accessed entry.
>
> Action: Craig to define this register
>
```

Tim
```
- ------- End of forwarded message -------

------- End of forwarded message -------
```

```
From:        wampler (Kurt Wampler)
Sent:        Monday, December 05, 1994 4:26 PM
To:          'geert'
Cc:          'hopper'; 'tbr'; 'vo'
Subject:     Re: Euterpe Route
```

Geert writes:
- - - - - - - - - - - -
> I would like to ask you to take responsibility for the Euterpe route
>for a while. I am too caught up in the placement to make any reasonable
>progress on the route.
>
> I woeked over the weekend on getting the euterpe snapshot in good
>sahpe so there is a good databse you can work from. There is currently
>a route running in the snapshot. It will be done later this afternoon.
>
> The snapshot gards directory will not change for a while. This is
>writable by anybody. You can also change the Makefiles in bsrc as long
>as you check them in immediately si that they get included in the next
>BOM.
>
> The snapshot is in :
>
>/n/auspex/s41/euterpe-snapshot/euterpe/verilog/bsrc

    OK - let me know when the current route is done and I'll pick it up from
    there. A 10-minute brain dump would be helpful too, when you have a chance.
    Simple questions like: is placement 100% complete now? including cerberus?
    and...what quality and completeness of result is expected at this point?

    - Kurt

From: geert (Geert Rosseel)

Sent: Tuesday, December 06, 1994 1:00 AM

To: 'billz'; 'brianl'; 'dickson'; 'geert'; 'hopper'; 'mws'; 'tbr'; 'woody'

Subject: Euterpe status

Hi,

Here is the state of the snapshot : Dec. 5

```
BLOCK       running     STATUS    BOM
         on
         machine

EUTERPE :                188.0

AU    :     FAILED TIMING  19.0
AT    :     BAD PLACEMENT  27.0
CC    :     FAILED TIMING  27.0
CDIO  :     O.K.        36.0
CJ    :     O.K.        78.0
CK    :     O.K.        18.0
CP    :     BAD PLACEMENT  24.0
CTIOD :     O.K.        14.0
CTIOI :     O.K.        13.0
DR    :     O.K.        45.0
DRIO  :     O.K.        11.0
ES    :     FAILED TIMING  68.0
GF    :     O.K.        21.0
GT    :     BAD PLACEMENT  60.0
HC    :     BAD PLACEMENT  65.0
HZ    :     O.K        10.0
ICC   :     BAD PLACEMENT  15.0
IFE   :     BAD PLACEMENT  35.0
IO    :     O.K.        27.0
IQ    :     O.K.        48.0
LT    :     O.K.        72.0
MC    :     O.K.        47.0
MST   :     O.K.        28.0
NB    :     FAILED TIMING  88.0
RG    :     O.K.        86.0
RGXMIT :    O.K.        17.0
SR    :     O.K.        43.0
UU    :     NO PLACEMENT
XLU   :     O.K.        41.0
```

From: solo (John Campbell)

Sent: Tuesday, December 06, 1994 2:51 AM

To: 'solo'

Cc: 'hopper'; 'lisar'; 'tbr'; 'tom'

Subject: VerifyRun test

The following differences were noticed since Yesterday.
in /n/auspex/s24/solo/test/compass/vlsi.boo and check.list

CELLNAME pl_euh
2c2
< /u/chip/euterpe/proteus/compass/gardswarts/pl_euh_logic.ly   No   5-Dec-94 18:05:21 GMT

> /u/chip/euterpe/proteus/compass/gardswarts/pl_euh_logic.ly   No   17-Nov-94 18:52:05 GMT
42c42
< /u/chip/euterpe/proteus/compass/layouts/epllopamp2.ly   1.19 Dec 5 11:52:42 1994

> /u/chip/euterpe/proteus/compass/layouts/epllopamp2.ly   1.18 Mar 10 01:02:20 1994
46d45
< epllpdbuf.ly   Mismatch RCS = 1.4 release = 1.3

CELLNAME pl_eus
2c2
< /u/chip/euterpe/proteus/compass/gardswarts/pl_eus_logic.ly   No   5-Dec-94 18:05:50 GMT

> /u/chip/euterpe/proteus/compass/gardswarts/pl_eus_logic.ly   No   17-Nov-94 18:52:07 GMT
43c43
< /u/chip/euterpe/proteus/compass/layouts/epllopamp2.ly   1.19 Dec 5 11:52:42 1994

> /u/chip/euterpe/proteus/compass/layouts/epllopamp2.ly   1.18 Mar 10 01:02:20 1994
47d46
< epllpdbuf.ly   Mismatch RCS = 1.4 release = 1.3

CELLNAME iobyte
2c2
< /u/chip/euterpe/proteus/compass/gardswarts/ioquadstdc.ly   No   5-Dec-94 17:56:06 GMT

> /u/chip/euterpe/proteus/compass/gardswarts/ioquadstdc.ly   No   2-Nov-94 00:22:19 GMT
15c15
< /u/chip/euterpe/proteus/compass/layouts/epllbmult.ly   1.15 Dec 5 11:52:37 1994

> /u/chip/euterpe/proteus/compass/layouts/epllbmult.ly   1.14 May 7 01:04:32 1994
17c17
< /u/chip/euterpe/proteus/compass/layouts/epllopamp2.ly   1.19 Dec 5 11:52:42 1994

> /u/chip/euterpe/proteus/compass/layouts/epllopamp2.ly   1.18 Mar 10 01:02:20 1994
51c51
< /u/chip/euterpe/proteus/compass/layouts/ioquadpdfilt.ly   1.13 Dec 5 11:52:50 1994

> /u/chip/euterpe/proteus/compass/layouts/ioquadpdfilt.ly   1.12 Jan 4 12:44:58 1994

....

The following mismatches were found between the released Version
cell or sub cells and the Version found in RCS.
You may want to release the later version, maybe not.

epllpdbuf.ly   Mismatch RCS = 1.4 release = 1.3
epllpdbuf.ly   Mismatch RCS = 1.4 release = 1.3

....
The following layouts were run today. This means either a change in
the schematic or layout.

Lvslog:12/06/94 GMT ***running LVS from echidna pid 20426
Lvslog:12/06/94 GMT ***/n/auspex/s24/solo/test
Lvslog:12/06/94 07:30 GMT running lvs -drac L pl_euh vs   S pl_euh
Lvslog:12/06/94 07:38 GMT running lvs -drac L pl_eus vs   S pl_eus
Lvslog:12/06/94 07:52 GMT running lvs -drac L iobyte vs   S iobyte
Drclog:12/06/94 GMT ***running DRC from echidna pid 12440
Drclog:12/06/94 GMT ***/n/auspex/s24/solo/test
Drclog:12/06/94 03:08 GMT running DRC -drac   on pl_euh
Drclog:12/06/94 07:04 GMT running DRC -drac   on pl_eus
Drclog:12/06/94 07:08 GMT running DRC -drac   on iobyte

....
The following cells may have bad lvs results. Check it out.

.....Circuit DISCREPANCIES

.....Possible Pin Problems

pl_euh pins may not match

....
The following cells may have bad drc results. Check it out.

☐ ************ERROR pl_euh FAILED DRC DIFF
☐ ************ERROR pl_eus FAILED DRC DIFF

....
The following cells may have shorts or opens.

From: solo (John Campbell)

Sent: Tuesday, December 06, 1994 5:30 AM

To: 'solo'

Cc: 'hopper'; 'lisar'; 'tbr'; 'tom'; 'vo'

Subject: VerifyRun snap

The following differences were noticed since Yesterday.
in /n/auspex/s24/solo/snap/compass/vlsi.boo and check.list

CELLNAME pl_euh
2c2
< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/gardswarts/pl_euh_logic.ly No   5-Dec-94 18:33:49 GMT

> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/gardswarts/pl_euh_logic.ly No   27-Nov-94 09:17:56 GMT
43d42
< epllopamp2.ly   Mismatch RCS = 1.19 release = 1.18
47d45
< epllpdbuf.ly   Mismatch RCS = 1.4 release = 1.3

CELLNAME pl_eus
2c2
< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/gardswarts/pl_eus_logic.ly No   5-Dec-94 18:32:56 GMT

> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/gardswarts/pl_eus_logic.ly No   27-Nov-94 09:05:20 GMT
44d43
< epllopamp2.ly   Mismatch RCS = 1.19 release = 1.18
48d46
< epllpdbuf.ly   Mismatch RCS = 1.4 release = 1.3

CELLNAME iobyte
2c2
< /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/gardswarts/ioquadstdc.ly No   5-Dec-94 18:23:55 GMT

> /n/auspex/s41/euterpe-snapshot/euterpe/proteus/compass/gardswarts/ioquadstdc.ly No   27-Nov-94 09:00:14 GMT
16d15
< epllbmult.ly   Mismatch RCS = 1.15 release = 1.14
19d17
< epllopamp2.ly   Mismatch RCS = 1.19 release = 1.18
55d52
< ioquadpdfilt.ly   Mismatch RCS = 1.13 release = 1.12

....
The following mismatches were found between the released Version
cell or sub cells and the Version found in RCS.
You may want to release the later version, maybe not.

epllbmult.ly   Mismatch RCS = 1.15 release = 1.14
epllopamp2.ly   Mismatch RCS = 1.19 release = 1.18
ioffout.ly   Mismatch RCS = 1.9 release = 1.8
ioquadpdfilt.ly   Mismatch RCS = 1.13 release = 1.12
latchx1.ly   Mismatch RCS = 1.12 release = 1.10
epllopamp2.ly   Mismatch RCS = 1.19 release = 1.18
epllpdbuf.ly   Mismatch RCS = 1.4 release = 1.3

epllopamp2.ly   Mismatch RCS = 1.19 release = 1.18
epllpdbuf.ly   Mismatch RCS = 1.4 release = 1.3

....
The following layouts were run today. This means either a change in
the schematic or layout.

Lvslog:12/06/94 GMT ***running LVS from echidna pid 3733
Lvslog:12/06/94 GMT ***/n/auspex/s24/solo/snap
Lvslog:12/06/94 09:58 GMT running lvs -drac L pl_euh vs   S pl_euh
Lvslog:12/06/94 10:07 GMT running lvs -drac L pl_eus vs   S pl_eus
Lvslog:12/06/94 10:29 GMT running lvs -drac L iobyte vs   S iobyte
Drclog:12/06/94 GMT ***running DRC from echidna pid 1662
Drclog:12/06/94 GMT ***/n/auspex/s24/solo/snap
Drclog:12/06/94 09:18 GMT running DRC -drac   on pl_euh
Drclog:12/06/94 09:19 GMT running DRC -drac   on pl_eus
Drclog:12/06/94 09:24 GMT running DRC -drac   on iobyte

....
The following cells may have bad lvs results. Check it out.

.....Circuit DISCREPANCIES

Verify/pl_euh/pl_euh.compare/pl_euh.lvs
Verify/pl_eus/pl_eus.compare/pl_eus.lvs

.....Possible Pin Problems

scsof1 pins may not match
scsdm8bv3 pins may not match
scsdm16 pins may not match
scxbcgbfr0 pins may not match

....
The following cells may have bad drc results. Check it out.

☐ ************ERROR pl_euh FAILED DRC DIFF
☐ ************ERROR pl_eus FAILED DRC DIFF

....
The following cells may have shorts or opens.

From: hopper (Mark Hofmann)

Sent: Tuesday, December 06, 1994 11:35 AM

To: 'hardheads'

Subject: 5pm release PIM/PIF

Hi,

I released a change to some of the AWK hair involved in the
PIM -> PIF -> PIM pipeline. This fixes a bug seen with the GF section of
Euterpe. It should not affect anyone else.

Let me know if things go all funny,

-hopper

From: Lisa Robinson [lisar@godzilla]

Sent: Tuesday, December 06, 1994 1:00 PM

To: 'tbr@godzilla'

Subject: forwarded message from Gregg Lahti

------- Start of forwarded message -------
Status: RO
X-VM-v5-Data: ([nil nil nil nil nil nil nil nil nil]
    ["5682" "Mon" "5" "December" "94" "17:37:50" "MST" "Gregg Lahti" "lahti_g@karoshi.vlsi.com " nil "122" "an
apology from Intel's CEO re: Pentium" "^From:" nil nil "12"])
Return-Path: <lahti_g@karoshi.vlsi.com>
Received: from muse.microunity.com by gaea.microunity.com (4.1/muse1.3)
    id AA08152; Mon, 5 Dec 94 16:41:04 PST
Received: from peanuts.vlsi.com by muse.microunity.com (4.1/ericm1.1)
    id AA08517; Mon, 5 Dec 94 16:41:02 PST
Received: from vlsiphx by peanuts.vlsi.com (8.6.9/SMI4.1-UCB8.6.9/Perlotto-DeLong-080394)
    id QAA28780; Mon, 5 Dec 1994 16:38:31 -0800
Received: from karoshi.psdphx by vlsiphx (4.1/SMI-4.1/Perlotto-102494)
    id AA06485; Mon, 5 Dec 94 17:39:28 MST
Reply-To: lahti_g@karoshi.vlsi.com
Received: from cyberpunk.psdphx by karoshi.psdphx (4.1/SMI-4.1)
    id AA13056; Mon, 5 Dec 94 17:37:50 MST
Message-Id: <9412060037.AA13056@karoshi.psdphx>
From: lahti_g@karoshi.vlsi.com (Gregg Lahti)
To: odell_d@karoshi.vlsi.com, davis_b@karoshi.vlsi.com, joet@primenet.com,
    laura@karoshi.vlsi.com, enterline@karoshi.vlsi.com,
    wood_c@karoshi.vlsi.com, barnes_m@karoshi.vlsi.com,
    jirgal_j@karoshi.vlsi.com, fall_b@karoshi.vlsi.com,
    thoman_j@karoshi.vlsi.com, donr@deico.com, bobek_r@karoshi.vlsi.com,
    jking@karoshi.vlsi.com, scotta@karoshi.vlsi.com,
    thomsen@ahi.geg.mot.com, cordes_c@phx.vlsi.com, earl@renmicro.com,
    doi@MicroUnity.com, lisar@MicroUnity.com, wombat@netcom.com,
    craw_m@phx.vlsi.com, LMcAndrew@aol.com, ohlfs_k@phx.vlsi.com,
    carlso_t@phx.vlsi.com, wild1@primenet.com, pesave_r@karoshi.vlsi.com,
    flanders@alice.macom.com, Yasushi_Matsushita@chdqm2.sps.mot.com,
    Robert_Johnson@chdqm2.sps.mot.com, kells_r@vlsiphx.vlsi.com,
    fishman@primenet.com, tam@alice.macom.com, mag@alice.macom.com,
    wilson_t@karoshi.vlsi.com, vance_c@phx.vlsi.com,
    dale_penner@spectrumsignal.bc.ca, srj@3com.com, bagnas_p@phx.vlsi.com,
    vogel_d@karoshi.vlsi.com, titan!mgoan@enuucp.eas.asu.edu,
    herring@netcom.com, casset_d@karoshi.vlsi.com, mcnees_s@phx.vlsi.com,
    garyh@karoshi.vlsi.com
Subject: an apology from Intel's CEO re: Pentium
Date: Mon, 5 Dec 94 17:37:50 MST

Forwarded from a friend, no posting header was contained.

    -Gregg

- ----- Begin Included Message -----

F

A posting from Intel:

This is Andy Grove, president of Intel. I'd like to comment a bit on
the conversations that have been taking place here.

First of all, I am truly sorry for the anxiety created among you by
our floating point issue. I read thru some of the postings and it's
clear that many of you have done a lot of work around it and
that some of you are very angry at us.

Let me give you my perspective on what has happened here.

The Pentium processor was introduced into the market in May of '93
after the most extensive testing program we at Intel have ever
embarked on. Because this chip is three times as complex as the 486,
and because it includes a number of improved floating point
algorithms, we geared up to do an array of tests, validation, and
verification that far exceeded anything we had ever done. So did many
of our OEM customers. We held the introduction of the chip several
months in order to give them more time to check out the chip and their
systems. We worked extensively with many software companies to this
end as well.

We were very pleased with the result. We ramped the processor faster
than any other in our history and encountered no significant problems
in the user community. Not that the chip was perfect; no chip ever
is. From time to time, we gathered up what problems we found and put
into production a new "stepping" -- a new set of masks that
incorporated whatever we corrected. Stepping N was better than
stepping N minus 1, which was better than stepping N minus 2. After
almost 25 years in the microprocessor business, I have come to the the
conclusion that no microprocessor is ever perfect; they just come
closer to perfection with each stepping. In the life of a typical
microprocessor, we go thru half a dozen or more such steppings.

Then, in the summer of '94, in the process of further testing (which
continued thru all this time and continues today), we came upon the
floating point error. We were puzzled as to why neither we nor anyone
else had encountered this earlier. We started a separate project,
including mathematicians and scientists who work for us in areas other
than the Pentium processor group to examine the nature of the problem
and its impact.

This group concluded after months of work that (1) an error is only
likely to occur at a frequency of the order of once in nine billion
random floating point divides, and that (2) this many divides in all
the programs they evaluated (which included many scientific
programs) would require elapsed times of use that would be longer than
the mean time to failure of the physical computer subsystems. In
other words, the error rate a user might see due to the floating point
problem would be swamped by other known computer failure mechanisms.
This explained why nobody -- not us, not our OEM customers, not the
software vendors we worked with and not the many individual users --
had run into it.

As some of you may recall, we had encountered thornier problems with
early versions of the 386 and 486, so we breathed a sigh of relief
that with the Pentium processor we had found what turned out to be a
problem of far lesser magnitude. We then incorporated the fix into
the next stepping of both the 60 and 66 and the 75/90/100 MHz Pentium
processor along with whatever else we were correcting in that next
stepping.

Then, last month Professor Nicely posted his observations about this
problem and the hubbub started. Interestingly, I understand from
press reports that Prof. Nicely was attempting to show that
Pentium-based computers can do the jobs of big time supercomputers in
numbers analyses. Many of you who posted comments are evidently also
involved in pretty heavy duty mathematical work.

That gets us to the present time and what we do about all this.

We would like to find all users of the Pentium processor who are
engaged in work involving heavy duty scientific/floating point
calculations and resolve their problem in the most appropriate fashion
including, if necessary, by replacing their chips with new ones. We
don't know how to set precise rules on this so we decided to do it
thru individual discussions between each of you and a technically
trained Intel person. We set up 800# lines for that purpose. It is
going to take us time to work thru the calls we are getting, but we
will work thru them. I would like to ask for your patience here.

Meanwhile, please don't be concerned that the passing of time will
deprive you of the opportunity to get your problem resolved -- we
will stand behind these chips for the life of your computer.

Sorry to be so long-winded -- and again please accept my apologies
for the situation. We appreciate your interest in the Pentium
processor, and we remain dedicated to bringing it as close to
perfection as possible.

I will monitor your communications in the future -- forgive me if I
can't answer each of you individually.

Andy Grove

- ------- End Included Message -----

- ----- End Included Message -----

------- End of forwarded message -------

From: sysadm@gaea on behalf of Bob Morgan [bobm@MicroUnity.com]

Sent: Tuesday, December 06, 1994 3:02 PM

To: 'euterpe@gaea'

Hi,

Just a reminder that if you use "gmake book" to print
out a copy of the microarchitecture document, it will
print out to Attilla, the printer by tbr's office.
Somebody left a copy on my chair, but I didn't print
it out. So if you tried to print out a copy of the
book, but don't know where it went, I have it. Let me
know and I'll even hand deliver it.
Thanks,
Bob

hi geert,

just for a test, i ran the previous placement i had of NB (with 14 rows instead of 7 below the Exlax area and which does fit to the left of the 2nd clock spar.) It converged in 4 iterations. The results are in my ~hopper/chip/euterpe/verilog/bsrc/ng/gards area.

i realize this isn't a workable placement. it just seems that if you can hold it from crossing a clock spar the timing is much easier to make.

-mark

From: billz (Bill Zuravleff)
Sent: Tuesday, December 06, 1994 4:08 PM
To: 'dickson'; 'geert'; 'mws'; 'woody'
Subject: Re: Bad path in cc - nb

Yes, I see the problem. A fanout of 40 for a df signal ("highpriority"
signal
into nb). As this is 5pS over, and probably not the last path of its kind, can we do
nothing for the time being -- except for adding to the list of "to be fixed" -- and still
make progress place and routing euterpe at the chip level? If so, let's.
billz

At 11.00am as usual.

Please be prepared to talk to your Pandora Schedule.

Lisa R.

Tbr   Pandora Base System Architecture
                 Pandora Base Board Development
                 Mnemosyne Logic Design

Graham (Yves)   Pandora Mixed Signal System Architecture
                 (Pandora Mixed Signal Board Development)

Geert   Euterpe CMOS Design

Lisa R.   Pandora System Functional Verification
                 (Pandora Base Hardware Bringup and System Test)
                 (Pandora Mixed Signal Hardware Bringup and System Test)

Hopper   Mnemosyne Final Verification and Tapeout

Anh   Mnemosyne Fabrication

Mudge   Mnemosyne Wafer Test and Characterization

Jt   Pandora Mechanical Development
                 (Pandora Manufacturing)

Gmo   Pandora OSF Kernel Development
                 Pandora OSF Software Bringup

Abbott   Pandora Mixed Signal Support Development
                 (Pandora Mixed Signal Software Bringup)

Van Dyke   Pandora Compiler Development
                 Pandora Benchmark

Hi -

I got a Euterpe routing result today that looks encouraging. It routed to 99.49%
completion, and used the "comb" obstructions that limit M2 length during the 3-layer maze
phase.

The disconnect pattern is also encouraging. There are 3 main groups of nets that need to
be dealt with, and just a handful of others. If you have a few minutes tomorrow
(Wednesday) I'd like to have you take a quick look at the disconnect pattern. I peered in
your office this evening before I left, but you were engaged in an animated discussion
with Drew & Mouss, and it didn't seem appropriate to butt in.

I may be able to fix one set of disconnects by routing them first, but the others may
require conversion of differential to pseudo-differential in order to reduce horizontal
wiring congestion.

- Kurt

(Hopper mentioned that Sophie's got chicken pox; I hope she's feeling better soon. I had
them as a child, but my wife didn't. When our daughter Deanna got them, my wife came down
with them too. They were able to give Karen something ... acyclovir? ... which speeded up
the disease and made the symptoms quite mild. If you or your wife are at risk of catching
them, you would certainly want to get ahold of this medicine.)

From: tbe@MicroUnity.com

Sent: Wednesday, December 07, 1994 12:52 PM

To: 'arya'

Cc: 'hestia'

Subject: Re: minutes from final pcb review of 12/1

Was there an answer to this action (first part)? We already have the clamps, and although it looks like it'll be a while before they clamp any real Calliopes or Euterpes, I'd like to get them modified so they're ready when needed.

>
>11) An insulator needs to be added to the bottom of the Ca/Eu clamps, to
>mitigate risk of impairing performance or shorting to closely spaced
>capacitor pads, and to provide de-coupling for traces beneath the clamp.
>
>Action: Arya to specify thickness of insulator required (assume e of 4.8)
>
>Action: tbe to get clamps modified with bonded G10 layer of specified
>thickness.
>

Thanks,

-Tom

Tom Eich | tbe@microunity.com
MicroUnity Systems Engineering, Inc.|
255 Caspian Dr. Sunnyvale, CA 94089 |
(408)734-8100, (408)734-8136 fax |

From:	doi (Derek Iverson)
Sent:	Wednesday, December 07, 1994 1:19 PM
To:	'gmo'; 'guarino'; 'sandeep'; 'gregg'; 'wayne'; 'iimura'; 'jeffm'; 'doi'
Cc:	'lisar'; 'hestia'
Subject:	Software Bringup Meeting Minutes - December 7, 1994

```
              Software Bringup Meeting
              -----------------------
                   December 7, 1994

Next Meeting:      December 14 at 10:00 am.

Attendees:  jeffm, guarino, gregg, doi, sandeep, wayne


New Action Items
------------------------------------------------------------------------
-

Item:  SW simulator has to be updated to reflect the new event daemon
       space.
Who:   gmo
Status:     [12/07] New.

Item:  Once the SW simulator has been updated to reflect the new event
       daemon space, some software will have to be changed too.
Who:   jeffm, guarino, sandeep
Status:     [12/07] New.


Review of Action Items
------------------------------------------------------------------------
---

Item:  Define and implement a snapshot environment for the HW and SW
       simulators.
Who:   jeffm, gmo
Status:     [11/30] In progress

       Jeff is going to start the process off with an e-mail message
       summarizing the current thoughts on the subject.

Item:  Get the cycle count for oc-mem test that ran on the hardware
       simulator.
Who:   doi
Status:     [11/30] Done.

       The data has been removed (not enought filespace to keep all this
       stuff around) but lisar will notify us when the next run is complete.

Item:  What is dependent on SC within Euterpe? ROM & LEDs?
       Reads of cerberus registers?
Who:   wayne
Status:     [11/23] No progress.

       Everything.  We spent a few minutes talking about a way for the
       CBI device to supply a local clock (without requiring a read or
       write operation from the host) until SD goes low.  Then the
       host would look after the interface (clock on read or write)
       until it decided to enable the CBI supplied clock.

Item:  Continue trying to find either source code for parallel drivers
       or descriptions of hardware so we can write out own.
```

```
Who:    gmo   sgi machines
Who:    doi   sun machines
Who:    wayne HPIB driver source or HW desc. for either Sun or SGI.
Status:       [11/23] progress continues.

        Expect info about Sun drivers from Acclaim.
        Expect info about SGI drivers from another vendor.
        Wayne says that we can get driver source code for a GPIB board.

Item: Implement parallel port device drivers for sun and sgi.
Who:    sandeep, doi
Status:       on hold pending discussion of CBI at the Pandora Meeting (11/18)

        Jerry K. found a driver on the Linux machine that appeared
        to handle interrupt based transactions.

        On achilles (if you have an id on the machine) you can see
        the code on /usr/src/linux/drivers/net/plipc.


Item: Build scripting/UI capabilities above gdb for regression tests.
Who:    doi
Status:       on hold until the the boot, gdb boot stub, and virtual devices
        are complete. (estimated start date of 12/23)

Item: Create performance test plan
Who:    jeffm, guarino
Status:       [11/30] no progress

Item: Add Unix-like tests to software acceptance tests.
Who:    iimura
Status:       [11/30] In progress.

Item: Simulator needs to understand `reset'
Who:    gmo
Status:       [11/30] In progress.

Item: Implement and bring-up boot, gdb boot stub, and virtual device
        support on the software simulator.
Who:    sandeep/gmo
Status:       in progress (due 12/23)

        Very close to having /dev/host working.


General Discussion
---------------------------------------------------------------------------
-

Jeff reports that the nb load/use problem is fixed and being tested and that nb anti-use
and sync ops are next on Mark's queue.


Test Status
---------------------------------------------------------------------------
-

Jeffm found a bug in the scaffolding that caused the gtlb tests to fail.
He has implemented a fix and is testing the result.
```

> Item: What is dependent on SC within Euterpe? ROM & LEDs?
>   Reads of cerberus registers?
> Who: wayne
> Status: [11/23] No progress.

This is done, as was seen by the recent flurry of mail. SC controll all the CMOS
circuitry. The rest of conversation was, was there a simple hardware fix in the
CBI that wouldn't require the software to constantly issue reads. See below
for details.

>
>   Everything. We spent a few minutes talking about a way for the
>   CBI device to supply a local clock (without requiring a read or
>   write operation from the host) until SD goes low. Then the
>   host would look after the interface (clock on read or write)
>   until it decided to enable the CBI supplied clock.
>

From: woody (Jay Tomlinson)

Sent: Wednesday, December 07, 1994 3:08 PM

To: 'vanthof'

Cc: 'geert'; 'tbr'

Subject: topt error message

Dave,
I got the following error messages (complete file is
/u/chip/euterpe/verilog/bsrc/gt/gards/makerrs). It appears some bad data got
into the strength file. Any idea of how this bad data got in there?

Jay

****

ERROR! Instance UgtSnake/UspMtchLate/Usetrdy/u0 (basename: xborff16) is being set to basename xborff15 from
strength file at line 120.
     This is a very very bad thing to do!
****

****

ERROR! Instance UgtSnake/UspMtchLate/UselPrbi/u0 (basename: xborff6) is being set to basename xborff5 from strength
file at line 125.
     This is a very very bad thing to do!
****

****

ERROR! Instance UgtSnake/UspMtchLate/Usetrdy_8/u0 (basename: xbor11) is being set to basename xbor8 from strength
file at line 128.
     This is a very very bad thing to do!
****

From: vanthof (vant)

Sent: Wednesday, December 07, 1994 3:17 PM

To: 'Jay Tomlinson'

Cc: 'vanthof (Dave Van't Hof)'; 'geert (Geert Rosseel)'; 'tbr (Tim B. Robinson)'

Subject: Re: topt error message

Jay Tomlinson writes:
>
>Dave,
>I got the following error messages (complete file is
>/u/chip/euterpe/verilog/bsrc/gt/gards/makerrs). It appears some bad data got
>into the strength file. Any idea of how this bad data got in there?
>
>Jay

The problem here is the strength file being read is out of date for the
listed instances. The netlist says the first instance is an xborff16 but
the strength file for that instance thinks that cell is a xborff15.

Something changed somewhere in the netlist from an earlier run, or
this strength file is being read in from a smaller module into the top level
and it's out of data with respect to the netlist.

The thing to do is to recreate that strength file being read in.

Hope this helps.
Dave

>
>
>*******************
>
>ERROR! Instance UgtSnake/UspMtchLate/Usetrdy/u0 (basename: xborff16) is being set to basename xborff15 from
strength file at line 120.
>   This is a very very bad thing to do!
>*******************
>
>*******************
>
>ERROR! Instance UgtSnake/UspMtchLate/UselPrbi/u0 (basename: xborff6) is being set to basename xborff5 from strength
file at line 125.
>   This is a very very bad thing to do!
>*******************
>
>*******************
>
>ERROR! Instance UgtSnake/UspMtchLate/Usetrdy_8/u0 (basename: xbor11) is being set to basename xbor8 from strength
file at line 128.
>   This is a very very bad thing to do!
>*******************
>
>

--

Dave Van't Hof   vanthof@microunity.com   MicroUnity Systems Engineering, Inc.
255 Caspian Way, Sunnyvale, CA (408) 734-8100 X276   #include <std_disclaim.h>
Don't blame me, I didn't vote for him!

From: fwo (Fred Obermeier)
Sent: Wednesday, December 07, 1994 3:19 PM
To: 'hardheads'
Cc: 'fwo'
Subject: Addition to Makefile.defs

Hi,

I've added the CHIP macro to {euterpe,proteus,calliope}/Makefile.defs
so that csyn and celltest can pick up the corresponding set rules and technology
information.

Unless I hear objections, I'll do a releasebom of these 3 files at 5pm.
This change should only effect leafnet stuff.

Fred.

Tim B. Robinson wrote (on Wed Nov 30, to abbott, gmo, lisa, mws):

> Curtis Abbott wrote (on Tue Nov 29):

>> I was just talking with Mark & Lisa about this and thinking about it.
>> I'm concerned about the degree of inter-thread interference in the
>> contemplated implementation. For example, assume that all stores from
>> other threads are shut down during an atomic op. The duty cycle in a
>> tight spin lock could be more than 50%, meaning stores are completely
>> disabled for 50% of the time anyone is spinning. Note that spinning
>> on a lock is generally considered by software people to be a nice way
>> to implement an idle loop!

>> I looked at the currently checked in code and the spin lock primitives
>> are a tight loop on smas64ai surrounded by debugging code. So this
>> concern is not academic.

>> We clearly need to do something about this. There is already some
>> sram hazard detection; could this be extended to narrow the
>> inter-thread interference down to a 64-byte region? Alternatively,
>> software is going to have to rethink how they use the atomic ops.

> Isn't it conventional to use some sort of test and test and set in
> that case rather than just the single sync op (ie avoiding the sync op
> all together until there is reason to believe you would actually be
> able to grab the lock). That ought to eliminate the problem.

I haven't heard anything back on this, and got a ping from Mark today on it. What do you
think? I assume it means we'd replace the lock code by something like

```
    for (;;) {
        while(*lockword & MYLOCKBIT)
            ;
        t = store_mux_and_swap(MYLOCKBIT, MYLOCKBIT, *lockword);
        if ((t & MYLOCKBIT) == 0)
            break;
    }
```

Seems like a reasonable suggestion to me. I believe it solves my issue. There is an
issue that if we implement atomic ops in the contemplated way (shutting down all stores
for awhile), a rogue app could spin on any of the sync ops and cause the whole machine to
pretty much freeze up. This is already sort of true of ggfmul8, at least on a digital
cable box, so I wouldn't say it's a showstopper...

Comments?

- Curtis

From:	tbr
Sent:	Wednesday, December 07, 1994 4:46 PM
To:	'wayne (Wayne Freitas)'
Cc:	'wayne'
Subject:	Question on clocks (again)
Follow Up Flag:	Follow up
Flag Status:	Red

Wayne Freitas wrote (on Wed Dec 7):

X-Sun-Data-Type: text
X-Sun-Data-Description: text
X-Sun-Data-Name: text
X-Sun-Content-Lines: 17

Tim, this was in Calliope.doc. It indicates that Calliope receives the Hermes
Clock from Euterpe, but doesn't go beyond mentioning that the output clock
is more than a buffered input signal. I thought that the output was either
generated or used a DLL, is this the case, and could you or someone in your
group expand on this alittle more.

There is a DLL which establishes quadrature with respect to the Hermes
input clock. This allws sampling of the data ate the centre of the
eye.

A buffered version of this quadrature clock is used to clock all the
circuitry at the outputboard side of the rate equalization fifos,
which includes the output flops in the output side of iobyte.
The actual clock output from the chip is really a ninth data bit which
just happens to have a value which continuously changes between 1 and
0. ie, the buffered quadrature clock clocks a 9 bit wire output
register and one of the bits in this register drives the Hermes output
clock pin. This ensures zero skew between the output clock and the
output data.

Tim

From:	Sandeep Nijhawan [sandeep@dolphin]
Sent:	Wednesday, December 07, 1994 4:58 PM
To:	'Curtis Abbott'
Cc:	'gmo@tallis'; 'lisa@tallis'; 'sandeep@tallis'; 'euterpe@tallis'
Subject:	Re: atomic ops

Curtis Abbott wrote:
>
> I haven't heard anything back on this, and got a ping from Mark today
> on it. What do you think? I assume it means we'd replace the lock
> code by something like
>   for (;;) {
>   while(*lockword & MYLOCKBIT)
>   ;
>   t = store_mux_and_swap(MYLOCKBIT, MYLOCKBIT, *lockword);
>   if ((t & MYLOCKBIT) == 0)
>   break;
>   }
> Seems like a reasonable suggestion to me. I believe it solves my
> issue. There is an issue that if we implement atomic ops in the
> contemplated way (shutting down all stores for awhile), a rogue app
> could spin on any of the sync ops and cause the whole machine to
> pretty much freeze up. This is already sort of true of ggfmul8, at
> least on a digital cable box, so I wouldn't say it's a showstopper...
>

     This is the first I've heard of this but the above looks reasonable.
It does make acquiring locks more expensive when there is no contention (which should be
true most of the time) but given the huge penalty of the smas implementation when there is
contention, we can (will have to) live with it.

     As far as mis-behaved apps are concerned the NB sub-system is another way such apps
can prevent other apps from working properly so I agree that

such sync instructions would hardly make things much worse.

Sandeep

From: ras (Bob Sutherland)

Sent: Wednesday, December 07, 1994 7:00 PM

To: 'ptolemy'

Subject: Minutes of 11/30 meeting

Hopefully this makes it out.

-ras showed some code capable of passing impedance information
accross a net. This was derived from brianl's work on a base
class set up to do this.

-brian completed work on an SDF socket and is in the process
of porting it to the DE domain. He showed some results of
information crossing between ptolemy and verilog.

At this point some conversation took place about networking a
system simulation as well as accelerating the simulation by compiling
to a floating-point DSP target. ras has the action to collect
information on S-bus and VME based solutions, with preference
toward the S-bus option.

Some further conversation occurred speculating about the
Zycad/IKOS interfacing and what would be the bottleneck.
brian has the action to build a complete PLL model across the
ptolemy/verilog interface, and we shall evaluate the Zycad
effect when this is available.

-Graham expressed some concern about improving the mechanism
for generating peicewise-linear behavioral models. ras
explained that what was being requested was an LMS
curve-fitting operation that ptolemy could readily perform
with some structuring. he now has the action to help dane
when this is needed.

-The action to provide a concept/ptolemy interface through
edif was discussed in absentia (brianl). In discussion after
the meeting it was determined that ras owed him some data in
ptolemy and concept (1:1 mapping). This has been provided.
brianl has the action to implement the preliminary conversion
path, which will then be optimized.

The next meeting is scheduled for 12/14 at 2:00 pm in the War room.

--
"No!No!.. Don't pull on that.. you never know what it's attached to."

RAS

From:	woody (Jay Tomlinson)
Sent:	Wednesday, December 07, 1994 7:11 PM
To:	'geert'
Subject:	forwarded message from Buffalo Chip

```
------- Start of forwarded message -------
Return-Path: <chip>
Received: from gamorra.microunity.com by gaea.microunity.com (4.1/muse1.3)
        id AA29649; Wed, 7 Dec 94 16:58:52 PST
Received: from localhost by gamorra.microunity.com (8.6.4/muse-sw.3)
        id QAA00533; Wed, 7 Dec 1994 16:58:49 -0800
Message-Id: <199412080058.QAA00533@gamorra.microunity.com>
From: chip (Buffalo Chip)
To: woody
Subject: output of euterpe/verilog/bsrc/gt/.checkoutrc
Date: Wed, 7 Dec 1994 16:58:49 -0800

The output from euterpe/verilog/bsrc/gt/.checkoutrc is 312k, so it is not included in this
mail message.  Instead, check the file

/n/tmp/chiplog/woody.gamorra.25659.euterpe-verilog-bsrc-gt

(which is accessible from all machines).  This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.
------- End of forwarded message -------
```

From: solo (John Campbell)

Sent: Wednesday, December 07, 1994 10:45 PM

To: 'solo'

Cc: 'hopper'; 'lisar'; 'tbr'; 'tom'

Subject: VerifyRun test

The following differences were noticed since Yesterday.
in /n/auspex/s24/solo/test/compass/vlsi.boo and check.list

CELLNAME bgvrslv2
2c2
< /u/chip/euterpe/proteus/compass/layouts/bgvrslv2.ly   1.8   Dec 6 10:44:17 1994

> /u/chip/euterpe/proteus/compass/layouts/bgvrslv2.ly   1.7   May 20 07:38:33 1994

CELLNAME pl_euh
6c6
< /u/chip/euterpe/proteus/compass/layouts/bgvrslv2.ly   1.8   Dec 6 10:44:17 1994

> /u/chip/euterpe/proteus/compass/layouts/bgvrslv2.ly   1.7   May 20 07:38:33 1994
45c45,46
< /u/chip/euterpe/proteus/compass/layouts/epllpdbuf.ly   1.4   Dec 6 14:14:00 1994

> /u/chip/euterpe/proteus/compass/layouts/epllpdbuf.ly   1.3   Mar 11 13:39:08 1994
> epllpdbuf.ly   Mismatch RCS = 1.4 release = 1.3

CELLNAME pl_eus
6c6
< /u/chip/euterpe/proteus/compass/layouts/bgvrslv2.ly   1.8   Dec 6 10:44:17 1994

> /u/chip/euterpe/proteus/compass/layouts/bgvrslv2.ly   1.7   May 20 07:38:33 1994
46c46,47
< /u/chip/euterpe/proteus/compass/layouts/epllpdbuf.ly   1.4   Dec 6 14:14:00 1994

> /u/chip/euterpe/proteus/compass/layouts/epllpdbuf.ly   1.3   Mar 11 13:39:08 1994
> epllpdbuf.ly   Mismatch RCS = 1.4 release = 1.3

CELLNAME iobyte
110c110
< /u/chip/euterpe/proteus/compass/leaf/xbmux2dh8s.ly   No   8-Dec-94 2:05:52 GMT

> /u/chip/euterpe/proteus/compass/leaf/xbmux2dh8s.ly   No   2-Dec-94 0:15:44 GMT

....
The following mismatches were found between the released Version
cell or sub cells and the Version found in RCS.
You may want to release the later version, maybe not.

....
The following layouts were run today. This means either a change in
the schematic or layout.

Lvslog:12/08/94 GMT ***running LVS from echidna pid 5701
Lvslog:12/08/94 GMT ***/n/auspex/s24/solo/test
Lvslog:12/08/94 03:30 GMT running lvs -drac L pl_eus vs   S pl_eus
Lvslog:12/08/94 03:39 GMT running lvs -drac L scxbcgbfr0 vs   S scxbcgbfr0
Lvslog:12/08/94 03:43 GMT running lvs -drac L iobyte vs   S iobyte
Drclog:12/08/94 GMT ***running DRC from echidna pid 3665
Drclog:12/08/94 GMT ***/n/auspex/s24/solo/test
Drclog:12/08/94 03:08 GMT running DRC -drac   on pl_euh
Drclog:12/08/94 03:12 GMT running DRC -drac   on iobyte

....
The following cells may have bad lvs results. Check it out.

.....Circuit DISCREPANCIES

.....Possible Pin Problems

iobyte pins may not match

....
The following cells may have bad drc results. Check it out.

....
The following cells may have shorts or opens.

From: geert (Geert Rosseel)

Sent: Wednesday, December 07, 1994 11:20 PM

To: 'tbr'

Subject: topt.new on toplevel netlist

Hi Tim,

Is it possible for you to run topt.new on a toplevel netlist foe Euterpe.
I don't have a top-level netlist that includes everything.

Topt.new will flag all the cases of mux - ff that can be replaced by muxff
(left-overs from the old design style). Making this change should save some
area (muxff is smaller than mux + ff and we save an intrinsic delay).

Geert

Looks like the snapshot build died again. For some reason it tried to
run spice on staypuft:

```
echo end generate spice scsof1
end generate spice scsof1
echo start simulate-cap scsof1
start simulate-cap scsof1
cd /n/auspex/s23/euterpe-proteus-cp/custom/caps; \
CHIPROOT=/n/auspex/s23/euterpe-proteus-cp /n/auspex/s23/euterpe-proteus-cp/proteus/spice/misc/cap/simulate-load -ci -
O /n/auspex/s23/euterpe-proteus-cp/custom/dcload/scsof1.cur scsof1 scsof1.sp
Err: The -chip {ChipName} argument is missing. Assuming proteus.
/n/auspex/s23/euterpe-proteus-cp/proteus/spice/misc/cap/simulate-load error: staypuft is not a licensed spice machine
/n/auspex/s23/euterpe-proteus-cp/proteus/spice/misc/cap/simulate-load error: Can not make scsof1.cap. Please re-run on a machine
/n/auspex/s23/euterpe-proteus-cp/proteus/spice/misc/cap/simulate-load error: listed in /n/auspex/s23/euterpe-proteus-cp/proteus/spice/misc/spice_machines
gmake[2]: *** [/n/auspex/s23/euterpe-proteus-cp/custom/caps/scsof1.cap] Error 1
rm /n/auspex/s23/euterpe-proteus-cp/custom/caps/scsof1.sp
gmake[2]: Leaving directory `/N/auspex/root/s23/euterpe-proteus-cp/ged/sc'
gmake[1]: *** [default] Error 1
gmake[1]: Leaving directory `/N/auspex/root/s23/euterpe-proteus-cp/ged'
gmake: *** [proteusmake] Error 1
```

From:	tbr
Sent:	Wednesday, December 07, 1994 11:30 PM
To:	'geert (Geert Rosseel)'
Subject:	topt.new on toplevel netlist
Follow Up Flag:	Follow up
Flag Status:	Red

Geert Rosseel wrote (on Wed Dec 7):

Hi Tim,

Is it possible for you to run topt.new on a toplevel netlist foe Euterpe.
I don't have a top-level netlist that includes everything.

I have BOM 187.1. It's not quite the latest, but probably good enough
for a test.

Topt.new will flag all the cases of mux - ff that can be replaced by muxff
(left-overs from the old design style). Making this change should save some
area (muxff is smaller than mux + ff and we save an intrinsic delay).

Great idea!

Tim

Geert Rosseel wrote (on Wed Dec 7):

   Hi Tim,

   Is it possible for you to run topt.new on a toplevel netlist foe Euterpe.
   I don't have a top-level netlist that includes everything.

I have BOM 187.1. It's not quite the latest, but probably good enough for a test.

   Topt.new will flag all the cases of mux - ff that can be replaced by muxff
   (left-overs from the old design style). Making this change should save some
   area (muxff is smaller than mux + ff and we save an intrinsic delay).

Great idea!

Tim

From:	wampler (Kurt Wampler)
Sent:	Wednesday, December 07, 1994 11:46 PM
To:	'geert'
Subject:	Re: Euterpe routing

>I was talking to Tom Vo about the XLU route problem. We need to import the
>xlu-route from the lower-level into the top-level . That should make
>the route of the external bus a lot easier. Let's talk tomorrow on how
>to do that.

   Yes, even if I can get it to route to completion, it would be better to
   reproduce the XLU wiring pattern exactly if we can.

   The route I started earlier today is still running; it's 50% of the way
   through the final maze pass, and 99.42% complete with 356 missing
   connections so far. I'll have a look at the unroutes in the morning;
   9600 baud is pretty slow for a full-chip REDIT session.

   - Kurt

I have the following report:

Original Path state:
  nbwe/Uawe/u0   (xborff6dh12s 12S) . Oport: q_ad0ph IntDel: 91.10 net: awe   swg: dh delay: 37.00ps RC
delay: 0.00ps   lds: 2 pcap: 41.06ff cap: 73.10ff (fan)
    abuf/webufa0   (forced ealnf36s9x4a 36S)   Iport: D0_AD0PH IntDel: 87.65
    Time through Path: 215.76

Path After Optimization using cycle time of 924.00:
  nbwe/Uawe/u0   (xborff6dh2s 2S)   Oport: q_ad0ph IntDel: 147.60 net: awe   swg: dh delay: 224.37ps RC
delay: 0.00ps   lds: 2 pcap: 41.06ff cap: 73.10ff (fan)
    abuf/webufa0   (ealnf36s9x4a forced 36S)   Iport: D0_AD0PH IntDel: 87.65
    Time through Path: 459.62

Where this is the last message I can find showing a change in the
drive strength of nbwe/Uawe/u0, yet further down I see this driver
showing up as 12s still in the summary of power levesl:

  awe (AWE) port: q_ad0ph Lds: 2 Ld Cur: 20.19   OldDr Cur: 5.96   PrevDrSz: 12   NewDr Cur: 35.72
CalcDrvSz: 9   NewDrvSz: 12   WireDel: 34.30 xborff6dh12s (nbwe/Uawe/u0)

and

  nbwe/Uawe/u0   (xborff6dh12s) powered up from 0S

and it also shows up in the < 50ps list:

  awe   (AWE) drvr: xborff6dh12s   DrvSz: 12   delay: 34.30 RCdelay: 0.00 cap: 7.31033e-14   pincap:
4.10633e-14   lds: 2 drvs: 1 (fan)
  awe_N (AWE_N) drvr: xborff6dh12s   DrvSz: 12   delay: 34.30 RCdelay: 0.00 cap: 7.31033e-14   pincap:
4.10633e-14   lds: 2 drvs: 1 (fan)

The generated strength file also has this cell as 12s.

Any idea what's going on? (The files are in
~tbr/euterpe/verilog/bsrc/nb/gards/nb-pass1.*).

Tim

I have the following report:

    Original Path state:
        nbwe/Uawe/u0   (xborff6dh12s 12S)   Oport: q_ad0ph   IntDel:
91.10 net: awe   swg: dh   delay: 37.00ps   RC delay: 0.00ps
lds: 2   pcap: 41.06ff   cap: 73.10ff (fan)
        abuf/webufa0   (forced ealnf36s9x4a 36S)   Iport: D0_AD0PH
IntDel: 87.65
        Time through Path: 215.76

    Path After Optimization using cycle time of 924.00:
        nbwe/Uawe/u0   (xborff6dh2s 2S) Oport: q_ad0ph   IntDel:
147.60   net: awe   swg: dh   delay: 224.37ps   RC delay: 0.00ps
lds: 2   pcap: 41.06ff   cap: 73.10ff (fan)
        abuf/webufa0   (ealnf36s9x4a forced 36S)   Iport:
D0_AD0PH   IntDel: 87.65
        Time through Path: 459.62

Where this is the last message I can find showing a change in the drive strength of
nbwe/Uawe/u0, yet firther down I see this driver showing up as 12s still in the summary of
power levesl:

      awe (AWE)   port: q_ad0ph   Lds: 2   Ld Cur: 20.19   OldDr Cur: 5.96
PrevDrSz: 12   NewDr Cur: 35.72 CalcDrvSz: 9   NewDrvSz: 12
WireDel: 34.30   xborff6dh12s (nbwe/Uawe/u0)

and

      nbwe/Uawe/u0   (xborff6dh12s)   powered up from 0S

and it also shows up in the < 50ps list:

        awe   (AWE) drvr: xborff6dh12s   DrvSz: 12   delay:
34.30   RCdelay: 0.00   cap: 7.31033e-14 pincap: 4.10633e-14
lds: 2   drvs: 1 (fan)
        awe_N (AWE_N)   drvr: xborff6dh12s   DrvSz: 12   delay:
34.30   RCdelay: 0.00   cap: 7.31033e-14 pincap: 4.10633e-14
lds: 2   drvs: 1 (fan)

The generated strength file also has this cell as 12s.

Any idea what's going on? (The files are in ~tbr/euterpe/verilog/bsrc/nb/gards/nb-pass1.
*).

Tim

From:	hopper (Mark Hofmann)
Sent:	Thursday, December 08, 1994 12:37 AM
To:	'Tim B. Robinson'
Cc:	'geert (Geert Rosseel)'
Subject:	Re: NB exlax arrays

Tim B. Robinson writes:

> All the outputs of the exlax arrays seem to have very low loading (at
> least in pass1). Is there any opportunity to save atoms by making a
> lower powered output flop available?
>
> Here's a typical output:
>
>   dout<40>   (DOUT_91_40_93_) drvr: eam2ffdh16s11x2a
> DrvSz: 16   delay: 28.04   RCdelay: 0.00   cap: 7.10901e-14
> pincap: 2.30301e-14   lds: 3   drvs: 1 (fan)
>
> For some reason the topt report does not seem to include the full path
> of any of these outputs so I can't see what the rest of the path looks
> like.

Hmmm. Possibly.

I have full reports (for an NB configuration which makes timing but is too big) in
~hopper/chip/euterpe/verilog/bsrc/nb/gards

-hopper

From:	Geert Rosseel [geert@rhea]
Sent:	Thursday, December 08, 1994 1:02 AM
To:	'geert@rhea'
Subject:	pager log message

```
page from geert to geert:
pageme gmake geert_euterpegards start:Dec_07_22:51 end: Dec_07_23:00 exit
1
```

From:	tbr
Sent:	Thursday, December 08, 1994 2:12 AM
To:	'geert'
Subject:	top level stat file
Follow Up Flag:	Follow up
Flag Status:	Red

There is a stat file in
~tbr/euterpe/verilog/bsrc/gards/tbr_euterpe-pass1.stat

from a top level top run with topt.new. It's too big to read into my
editor, what are we looking for?

Tim

From:	Geert Rosseel [geert@rhea]
Sent:	Thursday, December 08, 1994 3:50 AM
To:	'geert@rhea'
Subject:	pager log, sender copy

```
page from geert to geert:
pageme gmake geert_euterpegards start:Dec_07_23:21 end: Dec_08_01:48 exit
1
```

From: solo (John Campbell)

Sent: Thursday, December 08, 1994 10:04 AM

To: 'solo'

Cc: 'hopper'; 'lisar'; 'tbr'; 'tom'

Subject: VerifyRun test

The following differences were noticed since Yesterday.
in /n/auspex/s24/solo/test/compass/vlsi.boo and short.list

CELLNAME iobyte
108,109c108,109
< /u/chip/euterpe/proteus/compass/leaf/xbbufdh8s.ly   No   8-Dec-94 6:39:02 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbc01df4s.ly   No   8-Dec-94 12:48:00 GMT

> /u/chip/euterpe/proteus/compass/leaf/xbbufdh8s.ly   No   2-Dec-94 5:11:36 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbc01df4s.ly   No   2-Dec-94 10:56:57 GMT

....
The following mismatches were found between the released Version
cell or sub cells and the Version found in RCS.
You may want to release the later version, maybe not.

....
The following layouts were run today. This means either a change in
the schematic or layout.

Lvslog:12/08/94 GMT ***running LVS from echidna pid 5701
Lvslog:12/08/94 GMT ***/n/auspex/s24/solo/test
Lvslog:12/08/94 03:30 GMT running lvs -drac L pl_eus vs   S pl_eus
Lvslog:12/08/94 03:39 GMT running lvs -drac L scxbcgbfr0 vs   S scxbcgbfr0
Lvslog:12/08/94 03:43 GMT running lvs -drac L iobyte vs   S iobyte
Lvslog:12/08/94 GMT ***running LVS from echidna pid 29377
Lvslog:12/08/94 GMT ***/n/auspex/s24/solo/test
Lvslog:12/08/94 15:55 GMT running lvs -drac L iobyte vs S iobyte
Drclog:12/08/94 GMT ***running DRC from echidna pid 3665
Drclog:12/08/94 GMT ***/n/auspex/s24/solo/test
Drclog:12/08/94 03:08 GMT running DRC -drac   on pl_euh
Drclog:12/08/94 03:12 GMT running DRC -drac   on iobyte
Drclog:12/08/94 GMT ***running DRC from echidna pid 29300
Drclog:12/08/94 GMT ***/n/auspex/s24/solo/test
Drclog:12/08/94 15:54 GMT running DRC -drac L iobyte

....
The following cells may have bad lvs results. Check it out.

.....Circuit DISCREPANCIES

.....Possible Pin Problems

iobyte pins may not match

....

The following cells may have bad drc results. Check it out.

Possible ERROR drc.iobyte may be stuck in queue or just slow

....

The following cells may have shorts or opens.

```
> DEMUX: demux mpeg1/roger PASSED, Output matches reference
```

```
< UTIL: test_queues FAILED
> UTIL: test_queues PASSED, Output matches reference
```

From: paulb (Paul Berry)

Sent: Thursday, December 08, 1994 11:32 AM

To: 'tbr'

Subject: Re: Working: Mnemosyne module

Probably everyone but me already knows this...

I am unclear at what level you mean "module"
--from the point of view of the customer
  (who plugs the modules together)
--or from the point of view of the manufacturer
  (who puts various combinations of things into
  the same box)

If each (Mnemosyne + its DRAM) is a module,
does that module have an independent power supply
or does it just connect to a common power supply
shared by all the modules in the box?

As I understand it, there are always the 4 Mnemosyne's
you mentioned (to provide memory to Euterpe).
There is also one Menomsyne for each PCI bus,
and one for the (optional) Hermes link to Hestia. Are these
also constructed from the Mnemosyne module?
For a Pandora configured with two PCI busses and
a Hermes link to Hestia, I'm up to seven Mnemosynes.

Is that seven modules?
I have this image of them all in a row like the seven dwarfs,
or perhaps clipped to a track like track lighting for the home...

From: hopper (Mark Hofmann)
Sent: Thursday, December 08, 1994 3:23 PM
To: 'geert (Geert Rosseel)'
Subject: work to do?

Hi Geert,

   I'm temporarily out of bugs. (People haven't tried the fixes I put in yet) So- is there a section of euterpe I should look at?

   -mark

Hi,

There are a few remaining classes of errors identified by Tim Robinson's last csyn run.
Could those reponsible for the following blocks make the appropriate changes?

Unconnected cell inputs on all addupdat_* instances 2 through 63. E.g.:
      input
          instance path: top.xctioiupdat1u2.addupdat_34
          cellname path: top.xbmuxff2dh2s   .d1_ad0ph
      topmost net
          instance path: top.addupdat_34
          cellname path: top.addupdat_34

Problem with use of cgeb: 1p signals connect to other 2p signals:
phi_a2p3c
          leaf connections:
          instance path: top.xio1uoutposelu5.phileast_a2p
          cellname path: top.scioffdf16s   .phi_a2p3c
          ...
          instance path: top.xclk   .xu102u105.ckrao_ad1ph
          cellname path: top.cgclockbias.cgeb   .ckfo_ad1phw
          ...

      Similarly:
      xu102u105.ckrao_ad1ph
      xu102u105.ckrao_ad1ph
      xu103u103.ckrbo_ad1ph
      xu103u103.ckrbo_bd1ph

Driver and receiver have incompatible swings: fullswing drives mos.
      input
          instance path: top.xifeuifepgszselu0.ceifepgszsel_abm_0
          cellname path: top.xbcmos2ecldf2s   .cin_abm
      driver
          instance path: top.xuzceifepgszsel0_abmu0.ceifepgszsel_abm_0
          cellname path: top.xbc01df2s   .logic1_ab0pf
      topmost nets
          instance path: top.ceifepgszsel_abm_0
          cellname path: top.ceifepgszsel_abm_0

      Similarly:
      ceifepgszsel_abm_* for 0 to 4

Thanks,
Fred.

From:	tbr
Sent:	Thursday, December 08, 1994 6:20 PM
To:	'paulb (Paul Berry)'
Subject:	Re: Working: Mnemosyne module
Follow Up Flag:	Follow up
Flag Status:	Red

Paul Berry wrote (on Thu Dec 8):

Probably everyone but me already knows this...

I am unclear at what level you mean "module"
--from the point of view of the customer
 (who plugs the modules together)

--or from the point of view of the manufacturer
 (who puts various combinations of things into
 the same box)

Hopefully we plug the modules together. The idea came up to get more
3 dimensional packaging. However, I'm now thinking of going much
further and trying to define some kind of "Hermes backplane".
Potentially we could then have mnemosyne, calliope, or euterpe modules
and mix and match to make different systems from the same base modules.

If each (Mnemosyne + its DRAM) is a module,
does that module have an independent power supply
or does it just connect to a common power supply
shared by all the modules in the box?

Probably shared PSU. Colling is also an issue. Fan per module may be needed.

As I understand it, there are always the 4 Mnemosyne's
you mentioned (to provide memory to Euterpe).

Could be less, but at lower performance. Would depend on the application.

There is also one Menomsyne for each PCI bus,
and one for the (optional) Hermes link to Hestia. Are these
also constructed from the Mnemosyne module?

We have not got that far.

For a Pandora configured with two PCI busses and
a Hermes link to Hestia, I'm up to seven Mnemosynes.

No, the idea would be to sprout 2 PCIs from one Mnemosyne.

Is that seven modules?
I have this image of them all in a row like the seven dwarfs,
or perhaps clipped to a track like track lighting for the home...

The you have as much idea as we do as to how we would actually make

this work! Keep the ideas comming. . .

Tim

From:	tbr
Sent:	Thursday, December 08, 1994 6:28 PM
To:	'tom (Tom Laidig)'
Cc:	'fwo (Fred Obermeier)'; 'geert (Geert Rosseel)'; 'hopper (Mark Hofmann)'; 'Lisa Robinson'; 'Thomas Laidig'
Subject:	mnemo snapshot... disk space
Follow Up Flag:	Follow up
Flag Status:	Red

Tom Laidig wrote (on Thu Dec 8):

> I understand we're preparing to set up a snapshot area for mnemo. Am
> I correct in assuming that we want space for a mnemo and another full
> copy of proteus? If so, how much space would we expect to need for
> this? For reference, the existing euterpe snapshot is currently using
> 1.60GB for the euterpe part and 970MB for the proteus part.

We should try to "do it right", which would imply another proteus as
well as for mnemo. However, given the rate of change of proteus right
now, I doubt it would stand still long enough to count as a snapshot.

> Another request on the disk space horizon is space for celltest results
> for 4 rcode values. Currently, the results for 1 rcode value are using
> around 300MB of the protues disk, so we're looking for 900MB more space.
> For convenience, I'd like to cut the whole celltest tree off and put it
> on another disk, which means we're looking for a block of 1.2GB.

Can you do another general audit of the main auspex partitions we are
using for all the non user directories? I hope we can hold out with
what we have on the auspex till sometime in january when we should be
able to get 9GB drives. If we have to add more before then it will be
painful because all slots are full and we would have to add another
storage processor and racks. Once the 9GB drives are available, we
expect to trade up old 1.2 (ish) GB drives and replace them.

Tim

From: tbr

Sent: Thursday, December 08, 1994 6:52 PM

To: 'ericm'

Subject: auspex space

Follow Up Flag: Follow up

Flag Status: Red

We will need more auspex space probably in january as we gear up for the mnemosyne tapeout. I am going to ask Mike to get a formal quote for some 9GB drives, to trade for old (1.2GB? drives). When I last spoke to Ted Simon, he said there would be at least a 4 week lead time.

Tim

From: solo (John Campbell)

Sent: Thursday, December 08, 1994 10:58 PM

To: 'solo'

Cc: 'hopper'; 'lisar'; 'tbr'; 'tom'

Subject: VerifyRun test

The following differences were noticed since Yesterday.
in /n/auspex/s24/solo/test/compass/vlsi.boo and check.list

CELLNAME pl_euh
130,155c130,155

```
< /u/chip/euterpe/proteus/compass/leaf/xbbufdf12s.ly        No    8-Dec-94 6:51:15 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbbufdh16s.ly        No    8-Dec-94 6:57:43 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbcmos2ecldf2s.ly      No    8-Dec-94 14:05:22 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbcmos2ecldf6s.ly      No    8-Dec-94 13:56:09 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbffdf4s.ly         No    8-Dec-94 7:03:12 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbffdf8s.ly         No    8-Dec-94 6:39:04 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbffdh8s.ly         No    8-Dec-94 6:48:26 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor2df12s.ly        No    8-Dec-94 6:35:04 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor2df2s.ly        No    8-Dec-94 5:46:53 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor2df4s.ly        No    8-Dec-94 6:07:26 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor2dh16s.ly        No    8-Dec-94 15:10:36 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor3df12s.ly        No    8-Dec-94 6:04:43 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor3df2s.ly        No    8-Dec-94 6:02:45 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor3df4s.ly        No    8-Dec-94 6:02:22 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor4df12s.ly        No    8-Dec-94 6:23:55 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor4df2s.ly        No    8-Dec-94 5:57:52 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor4df4s.ly        No    8-Dec-94 6:03:14 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor5df2s.ly        No    8-Dec-94 5:58:57 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor7df4s.ly        No    8-Dec-94 6:08:58 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor8df4s.ly        No    8-Dec-94 6:03:48 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborff2df16s.ly       No    8-Dec-94 12:04:56 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborff4df12s.ly       No    8-Dec-94 11:50:49 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborff4dh16s.ly       No    8-Dec-94 9:02:28 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborff5df8s.ly       No    8-Dec-94 11:41:10 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborff6df8s.ly       No    8-Dec-94 11:35:29 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborffb7df8s.ly       No    8-Dec-94 11:29:26 GMT
---
> /u/chip/euterpe/proteus/compass/leaf/xbbufdf12s.ly        No    2-Dec-94 5:33:09 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbbufdh16s.ly        No    2-Dec-94 5:43:20 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbcmos2ecldf2s.ly      No    2-Dec-94 12:25:37 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbcmos2ecldf6s.ly      No    2-Dec-94 12:02:31 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbffdf4s.ly         No    2-Dec-94 5:43:46 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbffdf8s.ly         No    2-Dec-94 5:22:04 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbffdh8s.ly         No    2-Dec-94 5:20:19 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor2df12s.ly        No    2-Dec-94 5:21:01 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor2df2s.ly        No    2-Dec-94 4:30:18 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor2df4s.ly        No    2-Dec-94 4:57:13 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor2dh16s.ly        No    2-Dec-94 4:20:31 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor3df12s.ly        No    2-Dec-94 4:47:23 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor3df2s.ly        No    2-Dec-94 4:53:13 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor3df4s.ly        No    2-Dec-94 4:39:11 GMT
```

```
> /u/chip/euterpe/proteus/compass/leaf/xbor4df12s.ly          No    2-Dec-94 5:10:48 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor4df2s.ly           No    2-Dec-94 4:35:20 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor4df4s.ly           No    2-Dec-94 4:09:03 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor5df2s.ly           No    2-Dec-94 4:04:57 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor7df4s.ly           No    2-Dec-94 4:58:31 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor8df4s.ly           No    2-Dec-94 4:40:30 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborff2df16s.ly        No    2-Dec-94 10:33:24 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborff4df12s.ly        No    2-Dec-94 10:20:08 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborff4dh16s.ly        No    2-Dec-94 7:51:10 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborff5df8s.ly         No    2-Dec-94 8:59:11 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborff6df8s.ly         No    2-Dec-94 10:07:29 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborffb7df8s.ly        No    2-Dec-94 9:52:06 GMT

--------------------
CELLNAME pl_eus
135,161c135,161
< /u/chip/euterpe/proteus/compass/leaf/xbbufdf12s.ly          No    8-Dec-94 6:51:15 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbbufdf8s.ly           No    8-Dec-94 6:25:47 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbbufdh16s.ly          No    8-Dec-94 6:57:43 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbcmos2ecldf2s.ly        No    8-Dec-94 14:05:22 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbcmos2ecldf6s.ly        No    8-Dec-94 13:56:09 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbffdf4s.ly           No    8-Dec-94 7:03:12 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbffdf8s.ly           No    8-Dec-94 6:39:04 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbffdh8s.ly           No    8-Dec-94 6:48:26 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor2df12s.ly          No    8-Dec-94 6:35:04 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor2df2s.ly           No    8-Dec-94 5:46:53 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor2df4s.ly           No    8-Dec-94 6:07:26 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor2dh16s.ly          No    8-Dec-94 15:10:36 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor3df12s.ly          No    8-Dec-94 6:04:43 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor3df2s.ly           No    8-Dec-94 6:02:45 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor3df4s.ly           No    8-Dec-94 6:02:22 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor4df12s.ly          No    8-Dec-94 6:23:55 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor4df2s.ly           No    8-Dec-94 5:57:52 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor4df4s.ly           No    8-Dec-94 6:03:14 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor5df2s.ly           No    8-Dec-94 5:58:57 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor7df4s.ly           No    8-Dec-94 6:08:58 GMT
< /u/chip/euterpe/proteus/compass/leaf/xbor8df4s.ly           No    8-Dec-94 6:03:48 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborff2df32s.ly        No    8-Dec-94 12:39:25 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborff4df12s.ly        No    8-Dec-94 11:50:49 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborff4dh16s.ly        No    8-Dec-94 9:02:28 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborff5df8s.ly         No    8-Dec-94 11:41:10 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborff6df8s.ly         No    8-Dec-94 11:35:29 GMT
< /u/chip/euterpe/proteus/compass/leaf/xborffb7df8s.ly        No    8-Dec-94 11:29:26 GMT

---
> /u/chip/euterpe/proteus/compass/leaf/xbbufdf12s.ly          No    2-Dec-94 5:33:09 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbbufdf8s.ly           No    2-Dec-94 5:08:39 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbbufdh16s.ly          No    2-Dec-94 5:43:20 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbcmos2ecldf2s.ly        No    2-Dec-94 12:25:37 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbcmos2ecldf6s.ly        No    2-Dec-94 12:02:31 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbffdf4s.ly           No    2-Dec-94 5:43:46 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbffdf8s.ly           No    2-Dec-94 5:22:04 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbffdh8s.ly           No    2-Dec-94 5:20:19 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor2df12s.ly          No    2-Dec-94 5:21:01 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor2df2s.ly           No    2-Dec-94 4:30:18 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor2df4s.ly           No    2-Dec-94 4:57:13 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor2dh16s.ly          No    2-Dec-94 4:20:31 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor3df12s.ly          No    2-Dec-94 4:47:23 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor3df2s.ly           No    2-Dec-94 4:53:13 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor3df4s.ly           No    2-Dec-94 4:39:11 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor4df12s.ly          No    2-Dec-94 5:10:48 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor4df2s.ly           No    2-Dec-94 4:35:20 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor4df4s.ly           No    2-Dec-94 4:09:03 GMT
```

> /u/chip/euterpe/proteus/compass/leaf/xbor5df2s.ly	No	2-Dec-94 4:04:57 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor7df4s.ly	No	2-Dec-94 4:58:31 GMT
> /u/chip/euterpe/proteus/compass/leaf/xbor8df4s.ly	No	2-Dec-94 4:40:30 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborff2df32s.ly	No	2-Dec-94 10:01:27 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborff4df12s.ly	No	2-Dec-94 10:20:08 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborff4dh16s.ly	No	2-Dec-94 7:51:10 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborff5df8s.ly	No	2-Dec-94 8:59:11 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborff6df8s.ly	No	2-Dec-94 10:07:29 GMT
> /u/chip/euterpe/proteus/compass/leaf/xborffb7df8s.ly	No	2-Dec-94 9:52:06 GMT

CELLNAME xbc01df4s
6c6
< /u/chip/euterpe/proteus/compass/leaf/xbc01df4s.ly   No   8-Dec-94 12:48:00 GMT

> /u/chip/euterpe/proteus/compass/leaf/xbc01df4s.ly   No   2-Dec-94 10:56:57 GMT

....
The following mismatches were found between the released Version
cell or sub cells and the Version found in RCS.
You may want to release the later version, maybe not.

....
The following layouts were run today. This means either a change in
the schematic or layout.

Lvslog:12/09/94 GMT ***running LVS from echidna pid 18734
Lvslog:12/09/94 GMT ***/n/auspex/s24/solo/test
Lvslog:12/09/94 03:30 GMT running lvs -drac L pl_euh vs   S pl_euh
Lvslog:12/09/94 03:32 GMT running lvs -drac L pl_eus vs   S pl_eus
Lvslog:12/09/94 03:50 GMT running lvs -drac L xbc01df4s vs   S xbc01df4s
Lvslog:12/09/94 03:52 GMT running lvs -drac L iobyte vs   S iobyte
Drclog:12/09/94 GMT ***running DRC from echidna pid 16661
Drclog:12/09/94 GMT ***/n/auspex/s24/solo/test
Drclog:12/09/94 03:09 GMT running DRC -drac   on pl_euh
Drclog:12/09/94 03:10 GMT running DRC -drac   on pl_eus
Drclog:12/09/94 03:13 GMT running DRC -drac   on xbc01df4s

....
The following cells may have bad lvs results. Check it out.

.....Circuit DISCREPANCIES

.....Possible Other Problems

Did not find output file for cache.lvs
Did not find output file for cedmctrl_b.lvs
Did not find output file for cedmctrl_c.lvs
Did not find output file for cedmctrl_m.lvs
Did not find output file for cedmctrl_t.lvs

....
The following cells may have bad drc results. Check it out.

....
The following cells may have shorts or opens.

From: tbr (Tim B. Robinson)
Sent: Thursday, December 08, 1994 11:23 PM
To: 'euterpe'
Subject: News flash!

We just successfully ran the first program on Euterpe on the IKOS simulator.

Tim

From: vanthof (vant)

Sent: Thursday, December 08, 1994 11:39 PM

To: 'Tim B. Robinson'

Cc: 'vanthof (Dave Van't Hof)'; 'hopper (Mark Hofmann)'

Subject: Re: News flash!

Tim B. Robinson writes:
>
>We just successfully ran the first program on Euterpe on the IKOS
>simulator.
>
>Tim
>

Cool! How much faster was it than non-accelerated simulatoins????

--
Dave Van't Hof   vanthof@microunity.com   MicroUnity Systems Engineering, Inc.
255 Caspian Way, Sunnyvale, CA (408) 734-8100 X276   #include <std_disclaim.h>
Don't blame me, I didn't vote for him!

From: hopper (Mark Hofmann)

Sent: Friday, December 09, 1994 12:24 AM

To: 'Tim B. Robinson'

Subject: Re: News flash!

Tim B. Robinson writes:

> We just successfully ran the first program on Euterpe on the IKOS simulator.
>
> Tim

Great! So the latest vlit fixed things or did you need to patch around?

-hopper

From:	Tom Karzes [karzes@MicroUnity.com]
Sent:	Friday, December 09, 1994 3:26 AM
To:	'abbott@MicroUnity.com'
Cc:	'hayes@MicroUnity.com'; 'vandyke@MicroUnity.com'; 'gmo@MicroUnity.com'
Subject:	More changes to DES inner loop

In spite of what I said earlier, today I realized that I could shave off 2 more cycles
from the DES inner loop by avoiding the final consolidation of the intermediate result
into 64 bits and instead carrying the sparse 128-bit representation around the loop. This
eliminated a critical path XLU op and an associated stall. My current best version of the
loop runs in 30 cycles and has 2 stalls.

As far as the compiler issues go, nothing has really changed, except this time I was
forced to reassign registers in order to perform the reordering. It was still very easy
to do however.

Here's the original inner loop schedule generated by the compiler.
I believe this loop runs in 36 cycles (8 stalls):

```
    .LLB2:
            eshufflei4mux  r7,r6,r16,16,4,2
            l64l           r6,r3,r24
            etranspose8mux r7,r7,r11,r12
            gcopyswapi     r8,r8,127,16
            exor           r22,r7,r6
            euwthi         r18,r22,6,18
            euwthi         r7,r22,6,6
            euwthi         r6,r22,6,0
            euwthi         r19,r22,6,24
            euwthi         r21,r22,6,36
            euwthi         r15,r22,6,12
            euwthi         r20,r22,6,30
            euwthi         r22,r22,6,42
            lu8            r26,r2,r18
            eaddi          r24,r24,-8
            lu8            r27,r10,r22
            lu8            r18,r14,r7
            lu8            r22,r14,r6
            lu8            r23,r4,r19
            lu8            r6,r2,r15
            lu8            r7,r10,r21
            lu8            r19,r4,r20
            gmdepi64       r26,r6,4,0
            gmdepi64       r18,r22,4,0
            gmdepi64       r18,r26,8,8
            gxor           r8,r18,r8
            gselect8       r6,r9,r8,r5
            bgez           r24,.LLB2
```

Here's the same loop after reordering. Note that some registers were reassigned. I also
added comments where I expect stalls (which are all register dependencies). I believe
this loop runs in 30 cycles (2 stalls):

```
    .LLB2:
            eshufflei4mux  r7,r6,r16,16,4,2
            l64l           r6,r3,r24
            etranspose8mux r7,r7,r11,r12
            gcopyswapi     r8,r8,127,16
            exor           r15,r7,r6
            euwthi         r26,r15,6,18
            euwthi         r27,r15,6,42
            lu8            r26,r2,r26
            euwthi         r6,r15,6,12
            lu8            r27,r10,r27
```

```
            euwthi              r7,r15,6,36
            lu8                 r6,r2,r6
            euwthi              r18,r15,6,6
            lu8                 r7,r10,r7
            euwthi              r19,r15,6,30
            lu8                 r18,r14,r18
            euwthi              r22,r15,6,0
            lu8                 r19,r4,r19
            euwthi              r23,r15,6,24
            lu8                 r22,r14,r22
            gmdepi64            r26,r6,4,0
            lu8                 r23,r4,r23
            eaddi               r24,r24,-8
            gmdepi64            r18,r22,4,0
            /* stall */
            gmdepi64            r18,r26,8,8
            /* stall */
            gxor                r8,r18,r8
            gselect8            r6,r9,r8,r5
            bgez                r24,.LLB2
```

Finally, here's the C program I used as my starting point.   The inner loop is from the
second function in the file, "decrypt".

```
#include <types.h>
#include <terp/builtins.h>
#include <terp/c_extensions.h>
#include "crypt.h"

void
setkey(int padkey, crypt_key_t *crypt_key) {
    static  char    shifts[] = {
        1,1,2,2,2,2,2,2,1,2,2,2,2,2,2,1,
    };

    int     val;
    int     tmp1;
    int     tmp2;
    int     tmp3;
    int     i;
    int     k;

    /**
    *** Initial permutation to produce C and D (concatenated).
    *** The low-order bit of each byte is ignored.
    *** (from genperm < key_pc1.perm)
    **/

    tmp1 = eshufflei4mux(padkey, 0x33333333cccccccc5555aaaa5555aaaaLL,
                            16, 1, 8);

    tmp2 = etranspose8mux(tmp1, 0x0707717107077171,
                            0x1c6319661c63196655555a5a55555a5aLL);

    val = etranspose8mux(tmp2, 0x0055555555555555,
                            0x00f0f0f0f0f0f0f000cccc33333cccc3LL);

    /**
    *** To generate Ki, rotate C and D according
    *** to schedule and pick up a permutation
    *** using PC2.
    **/

    for (i = 0; i < 16; i++) {
        /**
        *** Rotate
        **/
```

```
        for (k = 0; k < shifts[i]; k++) {
            /**
            *** Rotate val left as two independent 28-bit pieces.
            *** (from genperm < key_rot.perm)
            **/

            tmp1 = eshufflei4mux(val,
0x00cccccccccccccc006a6a6a6aaaaaaaaLL,
                                        8, 1, 2);

            tmp2 = etranspose8mux(tmp1, 0x7068707070707070,

0x491c4c4c4c4c4c4c25522a2a2a2a2a2aLL);

            val = etranspose8mux(tmp2, 0x0099999999999999,

0x005555555555555500f0f0f0e1e1e1e1LL);
        }

        /**
        *** Permute to get this key value.
        *** Note that 8 bits are ignored.
        *** (from genperm < key_pc2.perm)
        **/

        tmp1 = e8mux(val, 0x00b494a452e0d0f0,
                        0x00c64c2834d0c698001ec1aa0e5285aaLL);

        tmp2 = etranspose8mux(tmp1, 0x3818383038383038,
                        0x0932152c0c252a0924290c1a26130915LL);

        tmp3 = etranspose8mux(tmp2, 0x00006347a3d2ac9c,
                        0x0000a97417e174d20000e42d39a696e4LL);

        /**
        *** Clear high 16 bits.  Note that it would be more efficient to
        *** clear the high 8 bits at the start, then use the permutations
        *** to leave the high 16 bits zero.  However, genperm currently
        *** can't handle this.
        **/

        crypt_key->keyvec[i] = tmp3 & 0x0000ffffffffffff;
    }
}

#define NO_COMPILER_IVS     1
#define EDFLAG              1

int
#if EDFLAG
decrypt(int data, const crypt_key_t *crypt_key) #else encrypt(int data, const crypt_key_t
*crypt_key) #endif {
    static ONCHIP unsigned char s01[64] = {
        239,  3, 65,253,216,116, 30, 71, 38,239,251, 34,179,216,132, 30,
         57,172,167, 96, 98,193,205,186, 92,150,144, 89,  5, 59,122,133,
         64,253, 30,200,231,138,139, 33,218, 67,100,159, 45, 20,177,114,
        245, 91,200,182,156, 55,118,236, 57,160,163,  5, 82,110, 15,217,
    };

    static ONCHIP unsigned char s23[64] = {
        167,221, 13,120,158, 11,227,149, 96, 54, 54, 79,249, 96, 90,163,
         17, 36,210,135,200, 82,117,236,187,193, 76,186, 36,254,143, 25,
        218, 19,102,175, 73,208,144,  6,140,106,251,145, 55,141, 13,120,
        191, 73, 17,244, 35,229,206, 59, 85,188,162, 87,232, 34,116,206,
    };

    static ONCHIP unsigned char s45[64] = {
         44,234,193,191, 74, 36, 31,194,121, 71,162,124,182,217,104, 21,
```

```
      128, 86, 93,   1, 51,253,244,174,222, 48,   7,155,229,131,155,104,
       73,180, 46,131, 31,194,181,124,162, 25,216,229,124, 47,131,218,
      247,107,144,254,196,   1, 90,151, 97,166, 61, 64, 11, 88,230, 61,
};

static ONCHIP unsigned char s67[64] = {
       77,209,178, 15, 40,189,228,120,246, 74, 15,147,139, 23,209,164,
       58,236,201, 53,147, 86,126,203, 85, 32,160,254,108,137, 23, 98,
       23, 98, 75,177,180,222,209,135,201, 20, 60, 74,126,168,226,125,
      160,159,246, 92,106,   9,141,240, 15,227, 83, 37,149, 54, 40,203,
};

int          val;
int128       val2;
int128       swapval2;
int          rrep;
int          tmp1;
int          tmp2;
int          stmp0x;
int          stmpx1;
int          stmp2x;
int          stmpx3;
int          stmp4x;
int          stmpx5;
int          stmp6x;
int          stmpx7;
int128       stmp0x_4x;
int128       stmpx1_x5;
int128       stmp2x_6x;
int128       stmpx3_x7;
int128       stmp01_45;
int128       stmp23_67;
int          i;

/**
*** Initial permutation, followed by the inverse of the inner loop
*** permutation (replicated on both halves).
*** (from genperm < ip_pinv.perm)
**/

tmp1 = eshufflei4mux(data, 0x333333c36ccc9ccc555555a5aaaa5aaaLL,
                           8, 1, 2);

tmp2 = etranspose8mux(tmp1, 0xd1711d17f0f00f0f,
                            0xe2362e639359399578e4874e556c55c6LL);

val = etranspose8mux(tmp2, 0x6395993963959939,
                           0x3af0ccb2c50f334db1a31ee8b1a31ee8LL);

/**
*** Initialize val2.
**/

val2 = gshufflei(0, val, 128, 16, 4);

/**
*** Initialize rrep.
**/

rrep = eselect8(val, 0x33221100);

/**
*** Perform an encryption operation 16 times.
***
*** Label the bytes of val as follows:
***
***      L0 L1 L2 L3 R0 R1 R2 R3
***
```

```
    *** The following values are live at the top of the loop:
    ***
    ***     val2 (128 bits):
    ***
    ***         0  0  0  0 L0 L1 R0 R1
    ***         0  0  0  0 L2 L3 R2 R3
    ***
    ***     rrep (64 bits):
    ***
    ***         R0 R0 R1 R1 R2 R2 R3 R3
    **/

#if EDFLAG
#if NO_COMPILER_IVS
    for (i = 120; i >= 0; i -= 8) {
#else
    for (i = 15; i >= 0; i--) {
#endif
#else
#if NO_COMPILER_IVS
    for (i = 0; i <= 120; i += 8) {
#else
    for (i = 0; i <= 15; i++) {
#endif
#endif
        /**
        *** Save the initial value with halves swapped
        **/

        swapval2 = gcopyswapi(val2, 0x7f, 0x10);

        /**
        *** Modified inner loop permutation, followed by expand.
        *** (from genperm < mod_p_e.perm)
        **/

        tmp1 = eshufflei4mux(rrep, 0x1c090e06182129221228031212302328LL,
                                   16, 4, 2);

        val = etranspose8mux(tmp1, 0x0000609653ea6aad,
                                   0x00003a3d597054f4000090fcabc0fc0eLL);

        /**
        *** XOR with key entry
        **/

#if NO_COMPILER_IVS
        val ^= *((int *) (((char *) crypt_key->keyvec) + i)); #else
        val ^= crypt_key->keyvec[i];
#endif

        /**
        *** Select
        **/

        stmp0x = s01[euwthi(val, 6, 42)];
        stmpx1 = s01[euwthi(val, 6, 36)];
        stmp2x = s23[euwthi(val, 6, 30)];
        stmpx3 = s23[euwthi(val, 6, 24)];
        stmp4x = s45[euwthi(val, 6, 18)];
        stmpx5 = s45[euwthi(val, 6, 12)];
        stmp6x = s67[euwthi(val, 6, 6)];
        stmpx7 = s67[euwthi(val, 6, 0)];

        stmp0x_4x = set_pair(stmp0x, stmp4x);
        stmpx1_x5 = set_pair(stmpx1, stmpx5);
        stmp2x_6x = set_pair(stmp2x, stmp6x);
        stmpx3_x7 = set_pair(stmpx3, stmpx7);
```

```
        stmp01_45 = gmdepi64(stmp0x_4x, stmpx1_x5, 4, 0);
        stmp23_67 = gmdepi64(stmp2x_6x, stmpx3_x7, 4, 0);

        val2 = gmdepi64(stmp23_67, stmp01_45, 8, 8);

        /**
        *** XOR with old swapped value
        **/

        val2 ^= swapval2;

        /**
        *** Combine and reorder in preparation for the next iteration.
        **/

        rrep = lo64(gselect8(hi64(val2), lo64(val2), 0x0000000099881100));
    }

    /**
    *** Consolidate value
    **/

    val = lo64(gshufflei(hi64(val2), lo64(val2), 128, 16, 2));

    /**
    *** Perform the inner loop permutation (replicated on both halves),
    *** swap halves, and perform the final permutation.
    *** (from genperm < p_fps.perm)
    **/

    tmp1 = eshufflei4mux(val, 0x99339999cc6633cc336655cc55aaaa66LL,
                             64, 1, 8);

    tmp2 = etranspose8mux(tmp1, 0xe8a5e1e1e8a5e1e1,
                                0x9ab8998d9ab8998da6d1b24ba6d1b24bLL);

    val = etranspose8mux(tmp2, 0xaaaaaaaaaaaaaaaa,
                               0x0f3333333cf00fc3ccc30fc3333cc3ccLL);

    return val;
}
```

From: hopper (Mark Hofmann)

Sent: Friday, December 09, 1994 4:35 AM

To: 'Bill Zuravleff'

Cc: 'tbr (Tim B. Robinson)'

Subject: Re: pim2pif failure

Bill Zuravleff writes:

hopper:
  What's this mean? (see ~billz/euterpe/verilog/bsrc/cc/gards/cc-pass1.pim.warn).

FATAL: /n/ghidra/s2/euterpe/tools/bin/pim2pif.ex [cgclockbias] has rail 538736
(not VSS/VDD)

You have an instance named cgclockbias:

cgclockbias   49   1

in your cc-pass1.pim file. This is the cuase of the error.
I suspect you may want to get rid of this line.

-hopper

From: tom (Tom Laidig)
Sent: Friday, December 09, 1994 9:40 AM
To: 'Tim B. Robinson'
Subject: Re: News flash!

Tim B. Robinson writes:
|
|We just successfully ran the first program on Euterpe on the IKOS
|simulator.

Cool! How fast did it run?

--
```
  ooooO  Ooooo
 ( _)  (_ )
  \( tau )/
  ()   ()
```

From: solo (John Campbell)

Sent: Friday, December 09, 1994 9:42 AM

To: 'Tim B. Robinson'

Cc: 'lisar (Lisa Robinson)'

Subject: Re: News flash!

as Tim B. Robinson was saying ....

..
..We just successfully ran the first program on Euterpe on the IKOS
..simulator.

..
..Tim

..
..

great job!

....
regards,
solo a.k.a. John Campbell   x516

```
>From Tim B. Robinson ...
@
@
@ Warren R. Ong wrote (on Tue Nov 15):
@    Yes, all of the exlax arrays will be re-simulated.  There is an
@    inherent race between the write wordline and the write bitlines.
@    We always want the write wordline to switch first.  I do not
@    anticipate any problems with rcd 6.
@
@ How easily can we verify we have no race at any code setting?  We @ certainly intend to
operate at code 1 in low power standby mode.
@
@    For euterpe, I only recall 2 arrays: nba16x64 and nbd32x64.  Are
@    there any others?
@
@ I think these are the only 2.
@
```

These two arrays have been spice with a resistor code of 1 and at 150MegHz. SPICE says
they are working correctly; edge rates of greater than 2ns have been seen, but there's
plenty of distance between edges.

I will do the same for buffer* when I know the definitive list of exlax cells for
menmosyne.

Warren.

From: geert (Geert Rosseel)
Sent: Friday, December 09, 1994 10:03 AM
To: 'vanthof'
Cc: 'hopper'; 'tbr'
Subject: Topt Core dump ... urgent

Hi Dave

I got twice a core file from topt : the result is in :

/u/geert/chip/euterpe/verilog/bsrc/mc

The makefile output is in :

/u/geert/chip/euterpe/verilog/bsrc/mc/make.out

The message I get is :

arning! Cell sccgbfr0 at line 56 is not in legal cell list
Warning! Cell sccgdr at line 98 is not in legal cell list
    Reading Cap/Delay table file /n/auspex/s14/geert/chip/euterpe/proteus/exlax/time/tim.lib

Connecting floating differential inputs to net vref_0ph...
    Connected 0 inputs to net vref_0ph...
Reading the drive strength file gards/mc-pass1.strength and setting power levels
/bin/sh: 22209 Memory fault - core dumped
gmake[2]: *** [gards/mc-pass2.sdl] Error 139
gmake[2]: Leaving directory `/N/auspex/root/s14/geert/chip/euterpe/verilog/bsrc/mc'
gmake[1]: *** [mc-base.netcap] Error 1
    ....

                    Geert

```
Geert Rosseel writes:
>
>
> Hi Dave
>
>I got twice a core file from topt : the result is in :
>
>/u/geert/chip/euterpe/verilog/bsrc/mc
>
>The makefile output is in :
>
>/u/geert/chip/euterpe/verilog/bsrc/mc/make.out

Will do, I'll look at it right away.
Dave
--
Dave Van't Hof   vanthof@microunity.com   MicroUnity Systems Engineering,
Inc.
255 Caspian Way, Sunnyvale, CA (408) 734-8100 X276   #include <std_disclaim.h> Don't blame
me, I didn't vote for him!
```

From:	tbr
Sent:	Friday, December 09, 1994 11:00 AM
To:	'vanthof (vant)'
Cc:	'hopper (Mark Hofmann)'; 'vanthof (Dave Van't Hof)'
Subject:	Re: News flash!
Follow Up Flag:	Follow up
Flag Status:	Red

vant wrote (on Thu Dec 8):

Tim B. Robinson writes:
>
>We just successfully ran the first program on Euterpe on the IKOS
>simulator.
>
>Tim
>

Cool! How much faster was it than non-accelerated simulatoins????

We have not measured performance carefully yet, but it's at least 20x
the Zycad speed which is in turn order 7x Verilog on the sparc 10,
so lets say around 150x. We have a way to go with performance tuning
though. We need to be around 25-30x zycad to meet the acceptance
criteria IKOS agreed to.

Tim

From: tbr
Sent: Friday, December 09, 1994 11:04 AM
To: 'hopper (Mark Hofmann)'
Subject: Re: News flash!
Follow Up Flag: Follow up
Flag Status: Red

Mark Hofmann wrote (on Fri Dec 9):

  Tim B. Robinson writes:

    We just successfully ran the first program on Euterpe on the IKOS
    simulator.

    Tim

  Great! So the latest vlit fixed things or did you need to patch around?

It fixed it. That seems to have been the last remaining problem.

Now we have to get the behavioral modeling working so we have an SDRAM . . .

Tim

From:	tbr
Sent:	Friday, December 09, 1994 11:06 AM
To:	'tom (Tom Laidig)'
Subject:	Re: News flash!
Follow Up Flag:	Follow up
Flag Status:	Red

Tom Laidig wrote (on Fri Dec 9):

> Tim B. Robinson writes:
>
> |
> |We just successfully ran the first program on Euterpe on the IKOS
> |simulator.
>
> Cool! How fast did it run?

Fast . . . Dunno quite how fast yet, but at least 20x Zycad.

Tim

geert

     in dickson/euterpe/verilog/bsrc/dr/gards is a first cut route of dr at left end of
data path. it didn't route at speed but it looks as tho it may fit in the last 1/2 clock
spar with a bit more work.

                       dickson

cc BOM 28.0 does not place.

OH YEAH? Well check out /u/chip/euterpe/verilog/bsrc/cc!
It's BOM 28.0 and it places *and* routes to completion.

(I'm presently working on the next (one-hot-state machine) version.
I will check in working placement soon -- within 2 hours -- unfortunately I don't think
I'll be able to get through icacheharder/dcacheharder within two hours, so it is still
likely to be buggy with respect to these tests.)

billz

```
/n/auspex/s41/euterpe-snapshot/euterpe/tools/bin/pim2pif: Processing the gards/cc-pas
s1.pim file...
/n/auspex/s41/euterpe-snapshot/euterpe/tools/bin/pim2pif.ex: FATAL: Errors encountere d in
.pim section 0, ...check log file `gards/cc-pass1.pim.warn'
/n/auspex/s41/euterpe-snapshot/euterpe/tools/bin/pim2pif.ex: FATAL: Errors occurred o n
some section(s) of the .pim file, ...check log file `gards/cc-pass1.pim.warn'
#pim2pif.ex Version 0.2.35 Fri Dec 9 06:19:03 PST 1994
foreach: No match.
gmake[2]: *** [gards/cc-pass1.pif] Error 1
gmake[2]: Leaving directory
`/N/auspex/root/s41/euterpe-snapshot/euterpe/verilog/bsrc
/cc'
gmake[1]: *** [cc-base.short.nets] Error 1 rm ccsm.esp ccstart.esp ccstart.optesp
ccsm.optesp
gmake[1]: Leaving directory
`/N/auspex/root/s41/euterpe-snapshot/euterpe/verilog/bsrc
/cc'
```

geert,
        i re-ran the dr block placed at the end of the data path because it core dumped last
nite. it converges in 5 iterations and routes at speed. in fact i talked to billz and its
10% smaller ??? if you want to look at it its at dickson/euterpe/verilog/bsrc/dr/gards it
does spill over the leftmost clock spar a bit but maybe it can be stretched a little bit
taller.

                        dickson

From:	vo (Tom Vo)
Sent:	Friday, December 09, 1994 7:39 PM
To:	'Geert Rosseel'
Cc:	'dickson (Richard Dickson)'; 'mws (Mark Semmelmeyer)'; 'tbr (Tim B. Robinson)'
Subject:	Re: rg does not place

```
Geert Rosseel wrote ....
>
>
> RG BOM 88.0 does not place. This one, I really need urgently ...
> Can someone look at this please. If you want to see what's wrong, you
>can look in the snapshot :
>
>   /n/auspex/s41/euterpe-snapshot/euterpe/verilog/bsrc/rg
>
>
>           Geert
>
```

I think you're picking up Rich's changes to fix the path to au . Rich made the *.V change
but did not get around to updating the placement . I believe that if you get an ealier rev
of rgdp.V (1.18) , rg would place again .

tvo

From: albers (Daniel Albers)

Sent: Friday, December 09, 1994 9:04 PM

To: 'albers (Daniel Albers)'; 'pmayer (Patricia Mayer)'; 'jt (John Tang)'; 'Tim B. Robinson'; 'Arya Behzad'; 'Philip Wong'

Cc: 'hopper (Mark Hofmann)'

Subject: main board vias/drill holes

Problem:

HADCO was seeing drill holes under VCO's, Euterpe, and Calliope which
would short power/gnd plans and cut through traces which we didn't
seem to know existed and we didn't catch in drc.

Cause:

We placed through-hole padstacks in some surface mount components to tie
them to ground. We used a through-hole because PCAD does not allow via
padstacks in components. We then neglected to create the corresponding
padstack. Therefore we didn't have any pads which would alert us to
drc violations or a drill symbol which would show up on the fab drawing.
PCAD of course reported the drill for the padstack in the excellon
drill table since it uses pin type (not padstack values) to determine
drill size.

Main Board Fix:

I will parse the pdif file and get a list of all pins which do not have
corresponding padstacks. We will use this information to fix the
main board. Patty is working on the layout of the internal layers to
work around the missing clearances. And we may have the vendor drop
some of the drill holes.

--
Daniel Albers   albers@microunity.com   MicroUnity Systems Engineering, Inc.
255 Caspian Way, Sunnyvale, CA (408) 734-8100

It can be made into a monster if we all pull together as a team...

Warren R. Ong wrote (on Fri Dec 9):

    >From Tim B. Robinson ...
    @
    @
    @ Warren R. Ong wrote (on Tue Nov 15):
    @   Yes, all of the exlax arrays will be re-simulated.   There is an
    @   inherent race between the write wordline and the write bitlines.
    @   We always want the write wordline to switch first.   I do not
    @   anticipate any problems with rcd 6.   .
    @
    @ How easily can we verify we have no race at any code setting?   We
    @ certainly intend to operate at code 1 in low power standby mode.
    @
    @   For euterpe, I only recall 2 arrays: nba16x64 and nbd32x64.   Are
    @   there any others?
    @
    @ I think these are the only 2.
    @

    These two arrays have been spice with a resistor code of 1 and at
    150MegHz.   SPICE says they are working correctly; edge rates of
    greater than 2ns have been seen, but there's plenty of distance
    between edges.

    I will do the same for buffer* when I know the definitive list of exlax
    cells for menmosyne.

Thanks.
Tim

From: arya (Arya Behzad)

Sent: Friday, December 09, 1994 9:30 PM

To: 'graham'

Cc: 'tbr'; 'mouss'; 'albers'

Subject: RE: VCO's on main PCB

>
> Agreed, the ground impedance should be as low as possible;
> ac components of the supply current, multiplied by ground impedance, would
> appear in series with the sensitive input tuning voltage, causing phase noise.
> Whether or not this becomes a problem is a matter of degree.
>
> However, I suspect everyone feels that we'll gain more benefit by recognizing
> that this fix is a compromise, enabling us to receive boards earlier for
> overall evaluation of other possible noise issues. The difficulties
> experienced with PCAD also dissuade us from database changes, until such time
> as replacement with Allegro occurs.
>
> Your thoughts, Arya?
> Graham.
> > From mouss@charybdis Fri Dec 9 16:29:22 1994
> > Date: 9 Dec 1994 16:30:07 -0800
> > From: "mouss" <mouss@charybdis>
> > Subject: RE: VCO's on main PCB
> > To: "Arya Behzad" <arya@charybdis>, "Graham Y. Mostyn" <graham@gaea>,
> >   "Tim B. Robinson" <tbr@gaea>
> > Content-Length: 1696
> >
> > Aren't VCO's sensitive to power supply noise, hence very much in need of low
> > impedance ground if we want to meet our jitter spec?!
> > _____
Hi,

Sorry for the late response. I have been in the lab starting the testing
on the daughter cards and I had not read my mail until now.

What Graham mentioned is exactly correct. We are aware of a few problems
with the current board layout. We are also certain that MANY issues will
have to be resolved once we start the testing process and find all the
unknown problems. Unfortunately, given out past experience with PCAD
and the fact that we are trying to switch as quickly as possible to Alegro,
it would have not made to much sense to delay the fabrication of the
board only to fix the VCO problems. The phase noise will be higher with
a higher impedance ground, but whether it will be large enough to cause
a problem is not clear. My mail was sent out on the understanding that
all the other problems that we had would be resolved by HADCO directly
and that it would not require us to redo the polygon entering process for the
internal layers and the resulting drc's which could easily take another
3 or 4 days (assuming no unanticipated problems from PCAD--a huge assumption).

I did not talk to Dan in detail since his return, but from his mail it sounds
like the problem is not specific to the VCO's and it actually occurs
under Calliope and Euterpe also, and therefore needs to be corrected. The VCO
vias will also then be fixed, I assume. Is this correct Dan?

Thanks.

-Arya

From:	tbr
Sent:	Saturday, December 10, 1994 12:20 AM
To:	'tom'
Subject:	shell question
Follow Up Flag:	Follow up
Flag Status:	Red

When invoking a command in a Makefile (using /bin/sh)
and setting the environment with:

a=b c=d doit

are you aware of any line length limit? I have the following case:

VOYAGER_HOME=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0
LM_LICENSE_FILE=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/voyager_license.dat IKOSTMP=ikostmp
IKOSCONF=/n/auspex/s15/tbr/euterpe/proteus/ikos IKOSLIB=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/lib
IKOSB=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/sys/etc
IKOSERR=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/sys/etc VOYAGER_MACHINE=sun_sparc
IKOSRAMTMP=ikostmp work=dls_work std=dls_std
dls_std=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/lib/vhdl/sun_sparc/std ikos=dls_ikos
dls_ikos=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/lib/vhdl/sun_sparc/ikos ieee=dls_ieee
dls_ieee=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/lib/vhdl/sun_sparc/ieee
PATH=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/bin/sun_sparc:$PATH /n/auspex/s15/tbr/euterpe/tools/vendoi
i_euterpe_wrap.vhdl

and this fails. To make it work I have to set the variable
VOYAGER_HOME explicitly in my environment before invoking the Make.

Tim

Hi,

Here is the status of the snapshot : Dec. 10


```
BLOCK           running          STATUS     BOM
                  on
                machine


EUTERPE      :                             191.0

AU      :            FAILED TIMING      20.0
AT      :            O.K.          28.0
CC      :            BAD PLACEMENT      28.0 (cc.pim 23.4)
CDIO    :            O.K.          36.0
CJ      :            O.K.          81.0
CK      :            O.K.          19.0
CP      :            BAD PLACEMENT      26.0
CTIOD   :            O.K.                  14.0
CTIOI   :            O.K.          13.0
DR      :            O.K.          45.0
DRIO    :            O.K.          11.0
ES      :            O.K           70.0
GF      :            O.K.          22.0
GT      :                O.K.          60.0
HC      :            O.K.          68.0
HZ      :            O.K           10.0
ICC     :            BAD PLACEMENT   16.0
IFE     :            BAD PLACEMENT      36.0
IO      :            O.K.          27.0
IQ      :            O.K.          48.0
LT      :            O.K.          72.0
MC      :            FAILED TIMING      47.0
MST     :            O.K.          28.0
NB      :            FAILED TIMING      88.0
RG      :            O.K.          88.0
RGXMIT      :            O.K.          17.0
SR      :                O.K.          43.0
UU      :            NO PLACEMENT
XLU     :            O.K.          41.0
```


                    Geert

From: mws (Mark Semmelmeyer)

Sent: Saturday, December 10, 1994 2:26 PM

To: 'euterpe-checkins-dist'; 'lisar'; 'tbr'; 'tom'

Subject: euterpe/verilog/bsrc/uu uuimmus.tdcd uuimmpcut.tdcd

Update of /p/cvsroot/euterpe/verilog/bsrc/uu
In directory medusa:/N/auspex/root/s24/mws/euterpe/verilog/bsrc/uu

Modified Files:
    uuimmus.tdcd uuimmpcut.tdcd
Log Message:
uu/uuimmpcut.tdcd: Operand prep codes for SN128WrIQ were not specified.
uu/uuimmus.tdcd: Immediate generation for SN128WrIQ not zeroing 14:4 for adrs.

From: tom (Tom Laidig)

Sent: Saturday, December 10, 1994 4:09 PM

To: 'Tim B. Robinson'

Cc: 'tom (Thomas Laidig)'

Subject: Re: shell question

Tim B. Robinson writes:
|
|
|When invoking a command in a Makefile (using /bin/sh)
|and setting the environment with:
|
|a=b c=d doit
|
|are you aware of any line length limit? I have the following case:
|
|VOYAGER_HOME=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0
LM_LICENSE_FILE=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/voyager_license.dat IKOSTMP=ikostmp
IKOSCONF=/n/auspex/s15/tbr/euterpe/proteus/ikos IKOSLIB=/n/auspex/s15/tbr/eute|rpe/tools/vendor/ikos/voyager_2.0/lib
IKOSB=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/sys/etc
IKOSERR=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/sys/etc VOYAGER_MACHINE=sun_sparc
IKOSRAMTMP=ikostmp work=dls_work std=dls_std
dls_|std=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/lib/vhdl/sun_sparc/std ikos=dls_ikos
dls_ikos=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/lib/vhdl/sun_sparc/ikos ieee=dls_ieee
dls_ieee=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/vo|yager_2.0/lib/vhdl/sun_sparc/ieee
PATH=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/bin/sun_sparc:$PATH /n/auspex/s15/tbr/euterpe/tools/vendo1
i_euterpe_wrap.vhdl
|
|and this fails. To make it work I have to set the variable
|VOYAGER_HOME explicitly in my environment before invoking the Make.

Ug. /bin/sh does have some limit, but I think it's much larger than
this. I checked with sysconf() on a sun, and found the limit for this
to be 1Meg. Then I cut and pasted this into a shell script, and added
FOO= and BAR= before the last two tokens (the command and its
argument), then added the command `printenv' at the end. It dutifully
put all the above stuff into the environment before running the
printenv command, which printed it all out. So I don't think /bin/sh is
the culprit. Perhaps gmake has some limit? One thing you might try is
to delay some of the expansion to the shell itself, perhaps by saying

```
IKOS=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos; \
VOYAGER_HOME=$IKOS/voyager_2.0 \
    LM_LICENSE_FILE=$IKOS/voyager_2.0/voyager_license.dat \
    IKOSTMP=ikostmp \
    IKOSCONF=$IKOS \
```

etc. This should cut down the number of characters involved in the call
of the shell from gmake.

```
--
 ooooO  Ooooo
 ( _) (_ )
 \( tau )/
 ( ) ( )
```

From:	tbr
Sent:	Saturday, December 10, 1994 4:44 PM
To:	'tom (Tom Laidig)'
Cc:	'tom (Thomas Laidig)'
Subject:	Re: shell question
Follow Up Flag:	Follow up
Flag Status:	Red

Tom Laidig wrote (on Sat Dec 10):

Tim B. Robinson writes:
|
|
|When invoking a command in a Makefile (using /bin/sh)
|and setting the environment with:
|
|a=b c=d doit
|
|are you aware of any line length limit? I have the following case:
|
|VOYAGER_HOME=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0
LM_LICENSE_FILE=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/voyager_license.dat IKOSTMP=ikostmp
IKOSCONF=/n/auspex/s15/tbr/euterpe/proteus/ikos IKOSLIB=/n/auspex/s15/tbr/eute|rpe/tools/vendor/ikos/voyager_2.0/lib
IKOSB=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/sys/etc
IKOSERR=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/sys/etc VOYAGER_MACHINE=sun_sparc
IKOSRAMTMP=ikostmp work=dls_work std=dls_std
dls_|std=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/lib/vhdl/sun_sparc/std ikos=dls_ikos
dls_ikos=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/lib/vhdl/sun_sparc/ikos ieee=dls_ieee
dls_ieee=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/vo|yager_2.0/lib/vhdl/sun_sparc/ieee
PATH=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/bin/sun_sparc:$PATH /n/auspex/s15/tbr/euterpe/tools/vendoi
i_euterpe_wrap.vhdl
|
|and this fails. To make it work I have to set the variable
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Ug. /bin/sh does have some limit, but I think it's much larger than
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printenv command, which printed it all out. So I don't think /bin/sh is
the culprit. Perhaps gmake has some limit? One thing you might try is
to delay some of the expansion to the shell itself, perhaps by saying

    IKOS=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos; \
    VOYAGER_HOME=$IKOS/voyager_2.0 \
        LM_LICENSE_FILE=$IKOS/voyager_2.0/voyager_license.dat \
        IKOSTMP=ikostmp \
        IKOSCONF=$IKOS \

etc. This should cut down the number of characters involved in the call
of the shell from gmake.

Thanks. I found it. The problem was confusion between VOYAGER_HOME
and IKOS_VOYAGER_HOME. However, I'm still not convinced there is no
problme, because whan I was trying to figure out what was going on
I did things liks

A=B printenv > foo; <doit>

and just putting the printenv in and out was making it say there was a
mismatched '

I'm baffled, but it's working now and so I'm not going to worry (well
at least not about that!)

Tim

From:	tom (Tom Laidig)
Sent:	Saturday, December 10, 1994 4:45 PM
To:	'Tim B. Robinson'
Cc:	'geert (Geert Rosseel)'; 'agc (Alan Corry)'; 'brianl (Brian Lee)'; 'lisar (Lisa Robinson)'; 'ong (Warren R. Ong)'; 'wampler (Kurt Wampler)'; 'doi (Derek Iverson)'
Subject:	Re: chipq

Tim B. Robinson writes:

> Geert Rosseel wrote (on Sat Dec 10):
>
> > Hi,
> >
> > Because of our machine dependencies in the chipq, a lot of stuff is
> > waiting in the queue that could start immediately. Maybe people can
> > kill their releases and start them up on another machine.
> >
> You should be able to start 2 on one machine, so you might get some
> going just by doing a chipq -noconflict

Actually, it's messier than that. vo's release in proteus (BOM 5.738, releasing only a
new version of Makefile.rules), seq# 2329, is waiting for brianl's leafgen release to
complete. But then all the other proteus jobs are waiting for it... I think.

Doi -- as far as I can tell, `chipq -t' only lists one reason why a job can't be run,
instead of all possible reasons. For example, chipq reported

```
   Seq# Target Directory                        Machine(pid)          Who
Stat
   ---- -----------------------------------     --------------------  --------
-----
 1 2326  proteus/leafgen                        ghidra(593)           brianl
29:01
 2 2329  proteus                                ghidra(11652)         vo
wait
 3 2338  proteus/compass/layouts                ares(18315)           ong
wait
 4 2343  proteus/ged/ea/ea1porl7nf8s3x4a        ares(19308)           ong
21:26
 5 2344  proteus/compass/layouts                clio(8149)            tom
wait
 6 2345  proteus/ged/gt                         clio(9649)            tom
wait
 7 2348  mnemo/verilog/src                      ares(24294)           agc
wait
 8 2353  euterpe/verilog/bsrc/cp                ghidra(2235)          brianl
wait
 9 2354  proteus                                rhodan(12235)         tbr
wait
10 2355  proteus/ikos                           aphrodite(7953)       tbr
wait
11 2356  proteus/compass/layouts                abderus(17546)        wampler
wait
12 2357  proteus/ikos/lib                       gamorra(28679)        tbr
wait
```

then I did a `chipq -d 2343' (the process had completed, but hadn't removed itself from
the queue for some reason). Then agc's release in mnemo/verilog/src fired off, and I get

```
   -clio:chipQ-> chipq -t 2338
   Sequence  : 2338
   Directory : proteus/compass/layouts
   Machine   : ares
   Who       : ong
```

There are already 1/1 jobs running on ares.

    NOT OK to run
    -clio:chipQ->

Clearly if that were the only problem, that job would have started before agc's job, whose
sequence number is 2348... ah! In fact, agc's job has now finished, and chipq now says

    -clio:chipQ-> chipq -t 2338
    Sequence : 2338
    Directory : proteus/compass/layouts
    Machine   : ares
    Who   : ong

    There is a conflict found for directory "proteus/compass/layouts"
    in the list of prior waiting jobs:
        proteus

    NOT OK to run
    -clio:chipQ->

Would it be possible for `chipq -t' to report all conflicts? This would make it much
easier to determine what jobs could be safely started by using `chipq -noconflict'.

Anyway, to relieve some of the constipation, I'm going to manually update
proteus/Makefile.rules and remove vo's entry from the chipq.

    --
        ooooO   Ooooo
        (_)   (_)
        \(~ tau ~)/
        (_)   (_)

From:	tbr (Tim B. Robinson)
Sent:	Monday, December 12, 1994 10:45 AM
To:	'mouss'; 'geert'; 'craig'
Subject:	CMOS euterpe

We never had the follow up discussion at the end of last week that got bumped from wednesday. Is there any opportunity this morning after 10 while Bulfer is in the orientation session? After that it's going to be hard to find a slot.

Tim

From: lisar (Lisa Robinson)

Sent: Monday, December 12, 1994 10:56 AM

To: 'jeffm'; 'mws'; 'woody'

Cc: 'tbr'

Subject: BOM 192

Well the verilog ran just fine. Is the force now really doing its job?

```
#ifdef RSTPCIBUF
initial begin
    force euterpe.rg.rgpc.z17C  = 1;
    force euterpe.rg.rgpc.z17C_N = 0;
end
#endif RSTPCIBUF
```


Or am I looking at a library problem. I'll re-run without the force.

Lisa R.

From:	Gregg Kellogg [gregg@hts.microunity.com]
Sent:	Monday, December 12, 1994 2:17 PM
To:	'lstein'; 'fur'; 'khp'
Subject:	cc-mode README

I found a cc-mode README file you guy's might be interested in:

README for cc-mode.el 4.85
Barry A. Warsaw <bwarsaw@cnri.reston.va.us> 1994/09/10 17:18:01

Note, you can browse this file either as a flat, multiple page file, or as an Emacs
outline. As a flat file, just use "C-x]" to move forward one page, or "C-x [" to move
backward one page. To read this as an outline, hit "M-x outline-mode RET". outline-mode
is described in your Emacs documentation.

* Introduction

    Welcome to cc-mode, version 4. This is a Emacs Lisp mode for
    editing C, C++, and Objective-C in GNU Emacs. This mode is
    decendent from c-mode.el (also called "Boring Old C Mode" or bocm
    :-), and c++-mode.el, version 2, which I have been maintaining
    since 1992. cc-mode represents a significant milestone in the
    mode's life. It has been fully merged back with Emacs 19's
    c-mode.el. Also a new, more intuitive and flexible mechanism for
    controlling indentation has been developed. More on this below.

    You can now use cc-mode to edit K&R and ANSI C, most ARM C++, and
    Objective-C programs. See below for limitations.

    In lieu of a texinfo manual (which is in the works -- volunteers
    are desperately sought!), this file will describe the following:

        * how to get started using cc-mode
        * how to customize the new indentation engine
        * the differences between cc-mode.el and bocm c-mode.el
        * the differences between cc-mode.el and c++-mode.el.

    Note that the name of the file is cc-mode.el, and I'll often refer
    to the mode as cc-mode, but there really is no top level cc-mode
    entry point. I call it cc-mode simply to differentiate it from
    c-mode.el. All of the variables, commands, and functions in
    cc-mode are prefixed with c-<thing>, and c-mode, c++-mode, and
    objc-mode entry points are provided. This file is intended to be
    a replacement for c-mode.el and c++-mode.el -- you should be able
    to remove them and dump Emacs with cc-mode.el instead. See the
    file DUMPING for details on how to do this.

    The major version number was incremented to 4 with the addition of
    objc-mode.

    This distribution contains release 4.85 of cc-mode. See below for
    a list of changes since the last release version 4.35. See the
    MANIFEST for a list of files that should have been included in
    this distribution.

    XEmacs 19.11 (formerly Lucid Emacs) now comes with cc-mode.el 4.85
    dumped in the executable. It has completely replaced c-mode.el
    and c++-mode.el. Both XEmacs and this distribution now contain a
    new file called cc-compat.el which should ease your transition
    from bocm to cc-mode. It comes unguaranteed and unsupported.

    Note also that I am moving to a new job! I don't yet know what
    the state of the mailing lists will be, but for a short while, I

expect mail will get forwarded to my new address, so please
continue to send bug reports, add/drop messages to the old
addresses. I'll make the appropriate announcements to the various
newsgroups when I know more what's going to happen. My
tentative new email address is given above. No guarantees that
will really be it, as I don't start the job until Sept. 19, 1994.
Don't try sending mail there at least until after that date.

* Getting Started

    cc-mode.el works well with the 2 main branches of Emacs 19, XEmacs
    (former Lucid Emacs) and the Emacs 19 maintained by the FSF.
    FSF's Emacs 19 users will want to use Emacs version 19.21 or
    better, XEmacs/Lucid users will want 19.6 or better. cc-mode.el
    works moderately well with Emacs 18, if you use the cc-mode-18.el
    compatibility file. A word of warning though, Emacs 18 lacks some
    fundamental functionality that makes Emacs 18 support a losing
    battle. Hence it is no longer supported and it is highly
    recommended that you upgrade to Emacs 19. If you use cc-mode
    under Emacs 18, you're on your own. With cc-mode version 5, Emacs
    18 support will be dropped altogether.

    The first thing you want to do is put cc-mode.el somewhere on your
    load-path where Emacs can find it. Do a "C-h v load-path" to see
    all the directories Emacs looks at when loading a file. If none
    of these directories are appropriate, create a new directory and
    add it to your load-path:

        [in the shell]
        % cd
        % mkdir mylisp
        % mv cc-mode.el mylisp
        % cd mylisp

        [in your .emacs file add]
        (setq load-path (cons "~/mylisp" load-path))

    Next you want to byte-compile cc-mode.el. The mode uses a lot of
    macros so if you don't byte-compile it, things will be unbearably
    slow. YOU CAN IGNORE ALL BYTE-COMPILER WARNINGS! They are the
    result of the multi-Emacs support and none of the warnings have
    any effect on operation. Let me say this again: YOU REALLY CAN
    IGNORE ALL BYTE-COMPILER WARNINGS!

    Here's what to do to byte-comple the file [in emacs]:

        M-x byte-compile-file RET ~/mylisp/cc-mode.el RET

    Most users will probably be running an Emacs that already has bocm
    c-mode.el dumped. You will not want to use this, or any older
    releases of c++-mode.el if you use cc-mode.el. If your Emacs is
    dumped with either of these files you first need to make Emacs
    "forget" about those older modes.

    If you can do a "C-h v c-mode-map" you probably need to add these
    lines at the top of your .emacs file:

        (fmakunbound 'c-mode)
        (makunbound 'c-mode-map)
        (fmakunbound 'c++-mode)
        (makunbound 'c++-mode-map)
        (makunbound 'c-style-alist)

    After those lines you will want to add the following autoloads to
    your .emacs file so that cc-mode gets loaded at the right time:

        (autoload 'c++-mode   "cc-mode" "C++ Editing Mode" t)

```
(autoload 'c-mode      "cc-mode" "C Editing Mode" t)
(autoload 'objc-mode "cc-mode" "Objective-C Editing Mode" t)
```

Important note: XEmacs 19.11 already have cc-mode.el dumped in
their Emacs, so if you are using that Emacs, do *not* add the
*makunbound or autoload lines above!

Next, you will want to set up Emacs so that it edits C files in
c-mode, C++ files in c++-mode, and Objective-C files in objc-mode.
All users (including XEmacs users) should add the following to
your .emacs file after the autoload lines above. Note that this
assumes you'll be editing .h and .c files as C, .hh, .C, and .cc
files as C++, and .m files as Objective-C. Your mileage may vary:

```
(setq auto-mode-alist
    (append '(("\\.C$"     . c++-mode)
              ("\\.cc$"    . c++-mode)
              ("\\.hh$"    . c++-mode)
              ("\\.c$"     . c-mode)
              ("\\.h$"     . c-mode)
              ("\\.m$"   . objc-mode)
        ) auto-mode-alist))
```

You may already have some or all of these settings on your
auto-mode-alist, but it won't hurt to put them on there again.

That's all you need. After you've done all this, you should quit
and restart Emacs. The next time you visit a C, C++, or
Objective-C file you should be using cc-mode. You can check this
easily by hitting "C-c C-v" in the c-mode, c++-mode, or objc-mode
buffer. You should see this message in the echo area:

       Using cc-mode version 4.85

* New indentation engine

    cc-mode has a new indentation engine, providing a simplified, yet
    flexible and general mechanism for customizing indentation. It
    breaks indentation calculation into two steps. First it tries to
    figure out what kind of language construct its looking at, then it
    applies a user defined offset to the current line based on the
    type of construct it finds.

    This section will briefly cover how indentation is calculated in
    cc-mode. Only enough detail will be given so that you will know
    how to customize indentation. Plenty of examples will be given to
    help you stylize your code, but more detailed examples will be
    left to the texinfo manual (when it is complete) and your own
    exploration. You can also contact the help address given below.

** Step 1: Syntactic Analysis

    In the first step, cc-mode looks at the line you are currently
    indenting and tries to determine the syntactic components of the
    construct on that line. cc-mode builds a list of these syntactic
    components, where each component on the list contains a "syntactic
    symbol" and a relative buffer position. Syntactic symbols
    describe elements of C/C++/Objc code such as `statement',
    `substatement', `class-open', `class-close', `knr-argdecl', etc.
    You can do a "C-h v c-offsets-alist" to see the entire list of
    support syntactic symbols along with a description of the
    constructs they represent.

    Conceptually, a line of C/C++/Objc code is always indented
    relative to the indentation of some line higher up in the buffer.
    This is represented by the relative buffer positions in the
    syntactic component list.

```

Here's an example. Suppose we had the following code in a c++-mode
buffer (the line numbers don't actually appear in the buffer):

Example 1:

```
1: void swap(int& a, int& b)
2: {
3:     int tmp = a;
4:     a = b;
5:     b = tmp;
6: }
```

We can use the command C-c C-s (c-show-syntactic-information) to
simply report what syntactic analysis is for a line.  If we hit
C-c C-s on line 4, we'd see in the echo area:

    ((statement . 36))

This tells us that the line is a statement and it is indented
relative to buffer position 36, which happens to be the `i' in
"int" on line 3.  If you were to move point to line 3 and hit C-c
C-s, you would see:

    ((defun-block-intro . 30))

This indicates that the `int' line is the first statement in a
block, and is indented relative to buffer position 30, which is
the brace just after the function header.

Here's another example:

Example 2:

```
1: int add( int val, int incr, int doit )
2: {
3:     if( doit )
4:         {
5:             return( val + incr );
6:         }
7:     return( val );
8: }
```

Hitting C-c C-s on line 4 gives us:

    ((substatement-open . 46))

which tells us that this is a brace that `opens' a substatement
block. By the way, a `substatement' indicates the line after an
if, else, while, do, switch, and for statements. See the variable
c-offsets-alist for a full description of the available syntactic
symbols.

Syntactic analysis lists can contain more than one element
(i.e. cons cell), and syntactic symbols need not have relative
buffer positions.

** Step 2: Indentation Calculation

Indentation for the current line is calculated using the list of
syntactic components derived in step 1 above. Each component
contributes to the final total indentation of the line in two
ways.

First, the syntactic symbol is looked up in the c-offsets-alist
variable, which is an association list of syntactic symbols and
the offsets to apply for those symbols. This offset is added to
the running total.

Second, if the component has a relative buffer position, cc-mode
adds the column number of that position to the running total. By
adding up the offsets and columns for every syntactic component on
the list, the final total indentation for the current line is
computed.

Lets use our two code examples above to see how this works. Just
as a reminder and a convenience the code is presented again here.

Example 1:

```
1: void swap( int& a, int& b )
2: {
3:     int tmp = a;
4:     a = b;
5:     b = tmp;
6: }
```

Lets say point is on line 3 and we hit the TAB key to re-indent
the line. Remember that the syntactic component list for that
line is:

    ((defun-block-intro . 30))

So first cc-mode is going to look up `defun-block-intro' in the
c-offsets-alist variable. Lets say it find the integer `4'; it
adds this to the running total (initialized to zero), yielding a
running total indentation of 4 spaces.

Next cc-mode goes to buffer position 30 and asks for the current
column. Since the brace at buffer position 30 is in column zero,
it adds 0 to the running total, and since there is only one
syntactic component on the list for this line, the total
indentation for the line is 4 spaces.

Example 2:

```
1: int add( int val, int incr, int doit )
2: {
3:     if( doit )
4:         {
5:             return( val + incr );
6:         }
7:     return( val );
8: }
```

If we were to hit TAB on line 4 in example 2 above, the same basic
process is performed, despite the differences in the syntactic
component list. Remember that the list for this line is:

    ((substatement-open . 46))

Here, cc-mode first looks up the `substatement-open' symbol in
c-offsets-alist, for which it might find `4'. At this point the
running total is 4 (0 + 4 = 4). cc-mode then goes to buffer
position 46, which is the `i' in "if" on line 3. This character
is in the fourth column on that line so adding this to the running
total, yields an indentation for the line of 8 spaces.

Simple, huh?

Actually, the mode usually just does The Right Thing without you
having to think about it in this much detail. But when
customizing indentation, its good to have a general idea of the
indentation model being used.

* Customizing Indentation

The c-offsets-alist variable is where you customize all your
indentations. You simply need to decide what additional offset
you want to add for every syntactic symbol. You can use the
command C-c C-o (c-set-offset) as the way to set offsets, both
interactively and from your mode hook. Also, you can set up
"styles" of indentation just like in standard c-mode.el. But
you'll probably find that most of the offsets are right for your
style.

In fact, the offset values in c-offsets-alist can be an integer, a
function or variable name, or one of the following symbols: +, -,
++, or --, indicating positive or negative multiples of the
variable c-basic-offset. Thus if you like the general indentation
levels, but you use 3 spaces instead of 4 spaces per level, you
can probably achieve your style by just changing c-basic-offset
like so (in your .emacs file):

        (setq c-basic-offset 3)

The offset value can also be a function, and this can really give
power users a lot of flexibility in customizing indentation.

As an example of how to customize indentation, lets change the
style of example 2 above from:

```
1: int add( int val, int incr, int doit )
2: {
3:     if( doit )
4:         {
5:             return( val + incr );
6:         }
7:     return( val );
8: }
```

to:

```
1: int add( int val, int incr, int doit )
2: {
3:     if( doit )
4:     {
5:         return( val + incr );
6:     }
7:     return( val );
8: }
```

Since line 4 is the start of the construct we want to re-indent,
we first move to that line and hit C-c C-s:

        ((substatement-open . 46))

So we know want to change the `substatement-open' indentation. To
do this interactively, just hit C-c C-o. This prompts you for the
syntactic symbol to change, giving you a reasonable default, in
this case, substatement-open, which is just the syntactic symbol
we want to change!

After you hit return cc-mode will then prompt you for the new
offset value, with the old value as the default. Hit backspace to
delete the old value, then hit "0" and then return. This moves
the construct one level of indentation to the left.

To check your changes quickly, just hit C-c C-q to reindent the
entire function. If this does what you want, you can put the
following lisp in your c-mode-common-hook (see below for an
example):

```
            (c-set-offset 'substatement-open 0)
```

You could also set up a "style" that sets this and all your
customizations in a convenient manner. See the variable
c-style-alist and the command c-set-style for more information, or
take a look at the sample .emacs file below.

* Frequently Asked Questions

        Q. How do I re-indent the whole file?
        A. Visit the file and hit "C-x h" to mark the whole buffer. Then
           hit "ESC C-\" to re-indent the entire region which you've just
           marked.

        Q. How do I re-indent the entire function? ESC C-x doesn't work
        A. ESC C-x is reserved for future Emacs use. To re-indent the
           entire function hit C-c C-q.

        Q. How do I re-indent the current block?
        A. First move to the brace which opens the block with "ESC C-u",
           then re-indent that expression with "ESC C-q".

        Q. Why doesn't the RET key indent the line to where the new text
           should go after inserting the newline?
        A. Emacs' convention is that RET just add a new line, and that LFD
           adds a newline and indents. You can make RET do this too by
           adding this to your c-mode-common-hook (see the sample .emacs
           file below):

           (define-key c-mode-map "\C-m" 'newline-and-indent)

           This is a very common question. :-) If you want this to be the
           default behavior, don't lobby me, lobby RMS!

        Q. I put (c-set-offset 'substatement-open 0) in my .emacs file and
           I get an error saying that c-set-offset's function definition is
           void.
        A. Since cc-mode is autoloaded, it is typically not loaded into
           your Emacs session by the time of the c-set-offset call.
           Instead of putting this in your top-level .emacs file, put the
           call to c-set-offset in your c-mode-common-hook. See the
           sample .emacs file below for details.

;; Sample .emacs file

;; Of course there are lots of other indentation features that I ;; haven't touched on
here. Until the texinfo is complete, you're ;; going to have to explore these on your
own. Here's a sample .emacs ;; file that might help you along the way. Just hit "C-x C-
p", then ;; "ESC w" to copy this region, then paste it into your .emacs file ;; with "C-
y". You may want to change some of the actual values.

(defconst my-c-style
  '("PERSONAL"
    (c-tab-always-indent   . t)
    (c-comment-only-line-offset   . 4)
    (c-hanging-braces-alist   . ((substatement-open after)
                                     (brace-list-open)))
    (c-hanging-colons-alist   . ((member-init-intro before)
                                     (inher-intro)
                                     (case-label after)
                                     (label after)
                                     (access-label after)))
    (c-cleanup-list   . (scope-operator
                                     empty-defun-braces
                                     defun-close-semi))
    (c-offsets-alist   . ((arglist-close   .
```

```
c-lineup-arglist)
                                          (substatement-open . 0
                                          (case-label        . 4)
                                          (block-open        . 0)
                                          (knr-argdecl-intro . -)))
     (c-echo-syntactic-information-p . t)
     )
  "My C Programming Style")

;; Customizations for both c-mode and c++-mode (defun my-c-mode-common-hook ()
  ;; set up for my perferred indentation style, but  only do it once
  (let ((my-style "PERSONAL"))
     (or (assoc my-style c-style-alist)
         (setq c-style-alist (cons my-c-style c-style-alist)))
     (c-set-style my-style))
  ;; offset customizations not in my-c-style
  (c-set-offset 'member-init-intro '++)
  ;; other customizations
  (setq tab-width 8
         ;; this will make sure spaces are used instead of tabs
         indent-tabs-mode nil)
  ;; we like auto-newline and hungry-delete
  (c-toggle-auto-hungry-state 1)
  ;; keybindings for C, C++, and Objective-C.  We can put these in
  ;; c-mode-map because c++-mode-map and objc-mode-map inherit it
  (define-key c-mode-map "\C-m" 'newline-and-indent)
  )

;; the following only works in Emacs 19
;; Emacs 18ers can use (setq c-mode-common-hook 'my-c-mode-common-hook) (add-hook 'c-mode-
common-hook 'my-c-mode-common-hook)
```

* User level differences between cc-mode.el and c-mode.el (as
  distributed with FSF Emacs 19.22).

    New indentation engine (described above).

    Direct support for C++ and Objective-C editing.

    Menubar support (Emacs 19 only).

    New variables:
        c-mode-common-hook
        c-strict-semantics-p
        c-echo-semantic-information-p
        c-basic-offset
        c-offsets-alist
        c-comment-only-line-offset
        c-block-comments-indent-p
        c-cleanup-list
        c-hanging-braces-alist
        c-hanging-colons-alist
        c-untame-characters (Emacs 18 users only)
        c-special-indent-hook
        c-delete-function
        c-electric-pound-behavior
        c-backscan-limit (Emacs 18 users only)

    Expanded semantics for variables:
        c-tab-always-indent
        c-style-alist

    New minor-mode features: auto-newline and hungry-delete-key (do
    "C-h f c-toggle-auto-hungry-state RET" for more info).

    New commands:
        c-toggle-auto-state   (C-c C-a)

```
      c-toggle-hungry-state           (C-c C-d)
      c-toggle-auto-hungry-state      (C-c C-t)
      c-electric-delete               (DEL)
      c-electric-slash                (/)
      c-electric-star                 (*)
      c-set-offset                    (C-c C-o)
      c-forward-into-nomenclature
      c-backward-into-nomenclature
      c-scope-operator
      c-tame-insert                   (Emacs 18 only)
      c-tame-comments                 (Emacs 18 only)
      c-indent-defun                  (C-c C-q)
      c-show-semantic-information     (C-c C-s)
      c-version                       (C-c C-v)
      c-submit-bug-report             (C-c C-b)

   Renamed commands:
      electric-c-brace        => c-electric-brace
      electric-c-semi         => c-electric-semi&comma
      electric-c-sharp-sign   => c-electric-pound
      mark-c-function         => c-mark-function
      electric-c-terminator   => c-electric-colon
      indent-c-exp            => c-indent-exp
      set-c-style             => c-set-style

   Obsolete variables:
      c-indent-level
      c-brace-imaginary-offset
      c-brace-offset
      c-argdecl-indent
      c-label-offset
      c-continued-statement-offset
      c-continued-brace-offset


* User level differences between cc-mode.el and c++-mode.el 2.353
  (a.k.a cplus-md1.el in FSF 19):

  New Indentation Engine (described above).

  General rename of all variables and defuns from c++-<thing> to
  c-<thing>.  I don't list them all individually here.

  Direct support for C and Objective-C editing.

  Menubar support (Emacs 19 only).

  New variables:
      c-strict-semantics-p
      c-echo-semantic-information-p
      c-basic-offset
      c-offsets-alist
      c-style-alist

  New commands:
      c-set-offset
      c-set-style
      c-fill-paragraph
      c-forward-into-nomenclature
      c-backward-into-nomenclature
      c-scope-operator
      c-beginning-of-statement
      c-end-of-statement
      c-up-conditional
      c-backward-conditional
      c-forward-conditional
      c-show-semantic-information
```

```
Other renamed commands/variables:
    c++-c-mode                    => c-mode
    c++-C-block-comments-indent-p => c-block-comments-indent-p
    c++-hanging-braces            => c-hanging-braces-alist
    c++-hanging-member-init-colon => c-hanging-colons-alist
    c++-default-macroize-column   => c-backslash-column
    c++-macroize-region           => c-backslash-region
    c++-electric-semi             => c-electric-semi&comma

Obsolete variables/commands:
    c++-always-arglist-indent-p
    c++-block-close-brace-offset
    c++-paren-as-block-close-p
    c++-continued-member-init-offset
    c++-member-init-indent
    c++-friend-offset
    c++-access-specifier-offset
    c++-empty-arglist-indent
    c++-auto-hungry-initial-state
    c++-auto-hungry-toggle
    c++-relative-offset-p
    c++-match-header-strongly
    c++-beginning-of-defun
    c++-end-of-defun
    c++-insert-header
    c++-match-paren
    c++-forward-sexp
    c++-backward-sexp
    c++-comment-region
    c++-uncomment-region
```

* For more information

    The best thing to do at this point is poke around the source code.
    Eventually there will be an extensive texinfo manual describing
    the mode in greater detail. Can I say this again? Volunteers to
    help finish the manual are desperately sought!

* Requirements

    cc-mode.el requires reporter.el for submission of bug reports.
    reporter.el is distributed with the latest FSF and Lucid Emacs
    19's. See below for Emacs Lisp Archive anonymous ftp'ing
    instructions for those of you who are using older Emacsen.

* Limitations and Known Bugs

    multi-line macros are not handled properly.

    re-indenting large regions or expressions can be slow.

    Use with Emacs 18 can be slow and annoying. You should seriously
    consider upgrading to Emacs 19.

    indentation of some nested switch constructs are known to be
    broken.

    there is still some weird behavior when filling C block comments.
    My suggestion is to check out add-on fill packages such as
    filladapt, available at the elisp archive.

* Electronic Mail

    To report bugs, use the C-c C-b (c-submit-bug-report) command.

This provides vital information I need to reproduce your problem.
Make sure you include a stripped down code example.

For other help or suggestions, send a message to
cc-mode-help@anthem.nlm.nih.gov.

To get on the beta testers list, send an add message to
cc-mode-victims-request@anthem.nlm.nih.gov. Note that this is a
fairly technical discussion list so you should be moderately Emacs
lisp fluent and have anonymous ftp access.

There is also an announce only list where you will get beta
version update diffs, but will not join in the technical
discussions. You should still have anon-ftp, and you shouldn't
expect beta releases to be as stable as public releases. Send an
add message to cc-mode-announce-request@anthem.nlm.nih.gov to be
added to this list.

Please use these addresses instead of my personal address so I can
keep track of all the incoming mail!

* Here's the Emacs Lisp Archive information for reporter.el:

        GNU Emacs Lisp Code Directory Apropos -- "reporter"
"~/" refers to archive.cis.ohio-state.edu:/pub/gnu/emacs/elisp-archive/

reporter (1.23)   02-Feb-1993
      Barry A. Warsaw, <bwarsaw@cen.com>
      ~/misc/reporter.el.Z
      Customizable bug reporting of lisp programs.

* User visible changes since 4.35

** c-set-offset and related functions and variables can now accept
   variable symbols. Also ++ and -- which mean 2* positive and
   negative c-basic-offset respectively.

** new variable, c-recognize-knr-p, which controls whether K&R C
   contructs will be recognized. Trying to recognize K&R constructs
   is a time hog so if you're programming strictly in ANSI C, set this
   variable to nil (it should already be nil in c++-mode).

** new variable, c-hanging-comment-ender-p for controlling
   c-fill-paragraph's behavior.

** new syntactic symbol: statement-case-open. This is assigned to
   lines containing an open brace just after a case/default label.

** new variable, c-progress-interval, which controls minibuffer update
   message displays during long re-indention. This is a new feature
   which prints percentage complete messages at specified intervals.

** Better menu titles in FSF's Emacs.

** Improved selective-display compatibility.

** Bug fixes, bug fixes, bug fixes!

** Some performance enhancements, but nothing radically better.

* User visible changes since 3.349

** New major-mode: objc-mode for Objective-C editing. Also added,
   objc-mode-hook, objc-mode-abbrev-table, objc-mode-map, and
   objc-mode-syntax-table.

** New syntactic symbols objc-method-intro, objc-method-args, and
   objc-method-call-cont have been added, with appropriate offsets in
   c-offsets-alist.

** Ellemtel style puts substatement-open braces on their own line.

** Better conformance to GNU coding style. New line up function set on
   arglist-close for GNU style: c-lineup-arglist-intro-after-paren.

** bracket lists are treated like paren lists (i.e. they are given the
   appropriate arglist-* syntax).

** some changes to recognition of brace-lists. When an otherwise
   brace-list-entry or brace-list-intro is found to start with an open
   brace, the line is given brace-list-open syntax instead.

** brace-list-intro and brace-list-entry are hangable via
   c-hanging-braces-alist.

** c-set-offset provides a reasonable default in the prompt.

** various name changes to commands and variables for consistency of
   terminology.   The changes are:

Cmd/Var	Old Name	New Name
[var]	c-strict-semantics-p	c-strict-syntax-p
[var]	c-echo-semantic-information-p	c-echo-syntactic-information-p
[var]	c-semantics	c-syntactic-context
[cmd]	c-show-syntactic-information	c-show-syntactic-information

   some other, non-user-level name changes were effected as well

** Usual gobs of bug fixes.

* User-visible Changes Since 3.304

** You can now specify `hanginess' of close braces. See
   c-hanging-braces-alist.

** New syntactic symbol `substatement-open' to control indentation of
   braces which open a substatement block (i.e. if, for, ...).   C-c
   C-s used to call these ((block-open . ??) (substatement . ??)), but
   now they are just ((substatement-open . ??)).   WARNING: THIS CHANGE
   MAY AFFECT YOUR CURRENT INDENTATION SETTINGS.

** c-adaptive-block-open lineup function is removed. Obsoleted by
   substatement-open change above.

** New "Default" style returns indentation variables to their default
   values.

** Support for Lucid Emacs 19.10's mode-popup-menu convention.

** c-macro-expand command put on C-c C-e.

** New buffer-local variable c-comment-start-regexp. Useful for using
   cc-mode as a basis for other C-like languages.

** c++-mode handles try/catch blocks.   Assigns them `substatement'
   syntax similar to if/for/while/...

** c-indent-via-language-element renamed to c-indent-line for
   awk-mode, BOCM compatibility.

** Usual gobs of bug fixes.

* User-visible Changes Since 3.229

** Tons 'o performance enhancements.

** Tons 'o bug fixes.

** Improved support for nested structs in C.

** Emacs 18 support has been split out into a separate file,
   cc-mode-18.el. Emacs 18 support is a losing battle, so after this
   release, I am not going to actively maintain cc-mode for Emacs 18,
   although I will incorporate contributed patches to cc-mode-18.el.

** The last of the dependencies on c-mode.el should be removed.

** New syntactic symbol, defun-block-intro, which controls the
   indentation for the first line in a top-level function or class.

** c-indent-defun moved to C-c C-q

** c-scope-operator moved to C-c :

** New coding style added to c-style-alist: Ellemtel. This supports
   the C++ coding style defined in "Programming in C++, Rules and
   Recommendations", Erik Nyquist and Mats Henricson, Ellemtel,
   ftp'able from euagate.eua.ericsson.se.

** c-set-style now modifies the global values by default. Buffer local
   versions are made when optional universal argument is given.

** New variable: c-inhibit-startup-warnings-p

** New custom indentation functions, which are not used by default:
   c-lineup-math and c-lineup-runin-statements. The former lines up
   math statement-cont lines after the equals sign. The latter lines
   up statement lines when the first statement in a block appears on
   the same line as the block opening brace.

From: geert (Geert Rosseel)

Sent: Monday, December 12, 1994 3:20 PM

To: 'billz'; 'brianl'; 'dickson'; 'geert'; 'hopper'; 'mws'; 'tbr'; 'vo'; 'woody'

Subject: Euterpe placement

Hi,

Here is the list :

Don't forget to update the latest *power.tab.top files.

hc0 :

$X0 = 160$
$Y0 = 476$

$XMAX < 620$
        Brian

nb :

top left of array :
$X0 = 620$
$Y0 = 456$

control of nb $XMAX < 1862$
wraps around array : top-left is limited by io0 : $XMIN > 498$
bottom is limited by mst : line (378, 437) -> (848, 437)
            xlu : line (848, 418) -> (1862, 418)

        Hopper

at :

right adjusted to :
$X0 = 1862$
$Y0 = 419$
Maximum $Y = 725$
        Jay

sr :

left adjusted

Datapath starts at
$X0 = 1915$
$Y0 = 476$ and is 64 bits high

Control logic under datapath
$X0 = 1915$ $XMAX < 2139$

Y0 > 419

       Brian

cc :

left adjusted to :

Datapath
  X0 = 1915
  YMAX = 668 and is 48 bits high

Control logic under datapath
  X0 = 2141
  YMIN = 476

       Billz

es :

What's happening with these larger gates in
the datapath.
  es/u00/u07/u220c/u0 to u7
  es/u00/u06/u220c/u0 to u7
  es/u00/u05/u220c/u7

These are 24s hr cells, all the other ones are 2s.

Is there any logical reason why they are different ?

      Rich

From:	geert (Geert Rosseel)
Sent:	Monday, December 12, 1994 3:58 PM
To:	'billz'; 'brianl'; 'dickson'; 'geert'; 'hopper'; 'mws'; 'tbr'; 'vo'; 'woody'
Subject:	Toplevel timing errors

```
Top-level timing errors :
  Use netcap for internal nets
  Use nof data for global nets


 stat file is :
/n/ghidra/s3/geert/euterpe/verilog/bsrc/gards/geert_euterpe-top.stat

********
nb to hcl
********


Warning!  Cycle time exceeded by 64.29ps using cycle time of 926.00 for
Iteration 1      HARD ERROR 1
    Path After Optimization using cycle time of 926.00:
        nb/nbprbarb/Ug2/u0        (xborffb6df32s 32S)      Oport: Q_ANDOPF
IntDel: 89.50    net: NBhclprgrant_N    swg: df delay: 383.40ps (force) RC
delay: 142.37ps       lds: 5  pcap: 38.11ff         cap: 571.72ff (ext)
m2len: 0.00  m3len: 4851.00  m4len: 0.00
        hcl/u420/Unst_2_2/u0      (xbor8df32s 32S)        Iport: D6_AOPF
Oport: Q_ANDOPF IntDel: 211.50 net: hcl/u420/nst_N_2_2 swg: df delay:
21.39ps (force)  RC delay: 0.71ps       lds: 3       pcap: 18.81ff
cap: 45.51ff (ext)  m2len: 0.00  m3len: 97.00  m4len: 170.00
        hcl/u420/Umuxen/u0        (xborff6dh12s 12S)              Iport:
D3_AOPF  IntDel: 284.50
        Time through Path: 990.29


**********
gt to at
********


Warning!  Cycle time exceeded by 77.59ps using cycle time of 926.00 for
Iteration 1      HARD ERROR 7
    Path After Optimization using cycle time of 926.00:
gt/UGtHitR10/u0 (xbffbdh24s 24S)        Oport: q_and0ph IntDel: 200.00
net: GIhitR10_N swg: dh delay: 355.84ps (force)      RC delay: 183.06ps
lds: 41 pcap: 264.62ff  cap: 740.48ff (ext)  m2len: 0.00  m3len: 4326.00
m4len: 0.00
        at/UatXcEnblR11/UilglAdrEn_0/u0 (xbor3df32s 32S)         Iport:
D0_AOPF  Oport: Q_ANDOPF IntDel: 165.00       net:
at/UatXcEnblR11/ilglAdrEn_N_0    swg: df delay: 10.56ps (force)  RC
delay: 0.29ps         lds: 1       pcap: 4.69ff     cap: 25.79ff (ext)
m2len: 0.00  m3len: 91.00  m4len: 120.00
        at/UatXcEnblR11/UilglAdrEn/u0   (xborff2df4s 4S)
Iport: D0_AOPF  IntDel: 272.20
        Time through Path: 1003.59

************
es to mst
************


Warning!  Cycle time exceeded by 37.35ps using cycle time of 926.00 for
Iteration 1      HARD ERROR 160
    Path After Optimization using cycle time of 926.00:
```

```
        es/u13/u0          (xbffbdh24s 24S)              Oport: q_ad0ph  IntDel:
88.20    net: EShotcarry swg: dh delay: 607.25ps (force)      RC delay:
394.35ps      lds: 1  pcap: 8.93ff     cap: 934.14ff (ext)  m2len: 0.00
m3len: 8411.00  m4len: 0.00
        mst/u00/u27/u0  (xbmuxff2dh12s 12S)              Iport: D0_AD0PH
IntDel: 267.90
        Time through Path: 963.35


*************
es to xlu
***********


Warning!  Cycle time exceeded by 134.90ps using cycle time of 926.00 for
Iteration 1     HARD ERROR 162
     Path After Optimization using cycle time of 926.00:
        es/u01/u00/u610/u7/u1   (xbffbdh24s 24S)         Oport: q_ad0ph
IntDel: 88.20    net: ESrsltR6_N<71>      swg: dh delay: 354.70ps
(force) RC delay: 202.67ps       lds: 1  pcap: 7.00ff    cap: 669.86ff
(ext)  m2len: 0.00  m3len: 6026.00  m4len: 0.00
        xlu/G_ctrldata/G_d_6ax_71       (sclp3 forced 33S)
Iport: din_and0ph       IntDel: 618.00
        Time through Path: 1060.90


*************
in es
***********


Warning!  Cycle time exceeded by 87.48ps using cycle time of 926.00 for
Iteration 1     HARD ERROR 318
     Path After Optimization using cycle time of 926.00:
        es/u00/u00/u163/u0      (xbmuxffb2df32s 32S)     Oport: Q_AND0PF
IntDel: 92.70    net: ESla_amountR3_N<3>     swg: df delay: 468.94ps
(force) RC delay: 242.91ps       lds: 2  pcap: 29.44ff   cap: 740.15ff
(ext)  m2len: 0.00  m3len: 6461.00  m4len: 0.00
        es/u00/u00/u200a/u3     (xbmux2dh16s 16S)        Iport: D0_AND0PH
Oport: q_and0ph IntDel: 65.00        net: es/u00/u00/edsum_n<3>      swg:
dh delay: 22.58ps (force)  RC delay: 0.93ps       lds: 3  pcap: 36.84ff
cap: 61.24ff (ext)  m2len: 0.00  m3len: 18.00  m4len: 226.00
        es/u00/u00/u200b/u3/u0  (xbmuxen2dh16s 16S)      Iport: D0_AND0PH
Oport: q_and0ph IntDel: 72.60        net: es/u00/u00/u200b/u3/m_N    swg:
dh delay: 4.86ps (force)   RC delay: 0.02ps       lds: 1  pcap: 7.52ff
cap: 12.42ff (ext)  m2len: 14.00  m3len: 7.00  m4len: 0.00
        es/u00/u00/u200b/u3/u1  (xbffdh8s 8S)            Iport: D0_ANDMPH
IntDel: 286.80
        Time through Path: 1013.48


*************
es to lt
***********


Warning!  Cycle time exceeded by 250.43ps using cycle time of 926.00 for
Iteration 1     HARD ERROR 512
     Path After Optimization using cycle time of 926.00:
        es/u00/u07/u200c/u7     (xbhrdh24s 24S) Oport: q_ad0ph  IntDel:
85.80    net: ESlvaR4R5<63>       swg: dh     delay: 803.83ps (force) RC
delay: 551.73ps      lds: 1  pcap: 7.52ff    cap: 1104.00ff (ext)  m2len:
0.00  m3len: 9968.00  m4len: 0.00
        lt/UesLvaR6/u16 (xbffdh2s 2S)               Iport: D0_ADMPH IntDel:
286.80
        Time through Path: 1176.43


        THESE ARE THE FEW LARGE GATES IN THE ES DATAPATH
```

```
**************
au to cdio
**************


Warning!  Cycle time exceeded by 19.11ps using cycle time of 926.00 for
Iteration 1      HARD ERROR 519
    Path After Optimization using cycle time of 926.00:
        au/ul12/u0      (xbmuxffb2dh24s 24S)      Oport: q_and0ph IntDel:
88.20    net: AUndx1500R2_N<6>    swg: dh      delay: 644.71ps (force) RC
delay: 422.26ps      lds: 5  pcap: 37.95ff    75.59ff (ext) m2len: 0.00
m3len: 8524.00  m4len: 0.00
        cdio/UrdNdxX3X4/u2      (xbhrdf8s forced 8S)      Iport:
D0_AND0PH      IntDel: 212.20
        Time through Path: 945.11



************
rg to au
************


Warning!  Cycle time exceeded by 158.03ps using cycle time of 926.00 for
Iteration 1      HARD ERROR 544
    Path After Optimization using cycle time of 926.00:
        rg/rg1/Uopb0R0/u0      (xbmuxffb2df32s 32S)      Oport: Q_AND0PF
IntDel: 92.70   net: RGopbR0_N<0>         swg: df delay: 421.18ps
(force) RC delay: 201.49ps      lds: 15 pcap: 148.86ff  cap: 718.55ff
(ext)  m2len: 0.00   m3len: 5179.00  m4len: 0.00
        au/u02a/u0      (xbor2df32s 32S)      Iport: D0_A0PF  Oport:
Q_AD0PF  IntDel: 164.20  net: au/ga_n<0>    swg: df delay: 98.75ps
(force)  RC delay: 12.17ps      lds: 7  pcap: 48.22ff    cap: 174.12ff
(ext)  m2len: 0.00  m3len: 598.00  m4len: 661.00
        au/u05a/u0      (xborff15df4s 4S)      Iport: D14_A0PF
IntDel: 307.20
        Time through Path: 1084.03



************
rg to es
************
Warning!  Cycle time exceeded by 39.29ps using cycle time of 926.00 for
Iteration 1      HARD ERROR 809
    Path After Optimization using cycle time of 926.00:
        rg/rg1/Uopb5R0/u0      (xbmuxffb2df32s 32S)      Oport: Q_AD0PF
IntDel: 91.50    net: RGopbR0<5> swg: df      delay: 545.79ps (force) RC
dela0.00  m3len: 5511.00  m4len: 0.00
        es/u00/u00/u19/u5      (xbmuxff3dh2s 2S)      Iport:
D1_AD0PH IntDel: 328.00
        Time through Path: 965.29



************
in hc1 : several similar errors
************


Warning!  Cycle time exceeded by 2.23ps using cycle time of 926.00 for
Iteration 1      HARD ERROR 923
    Path After Optimization using cycle time of 926.00:
        hc1/Uspsel1/u1  (xbffbdh24s 24S)      Oport: q_ad0ph  IntDel:
88.60    net: hc1/spsel1<1>      swg: dh      delay: 128.56ps (force) RC
delay: 47.89ps      lds: 32 pcap: 153.49ff  cap: 390.19ff (ext)  m2len:
0.00  m3len: 848.00  m4len: 1273.00
        hc1/Usadr/u3      (xbmux4dh16s 16S)      Iport: SEL_A0PEH<1>
Oport: q_ad0ph  IntDel: 117.90  net: hc1/sadr<3>    swg: dh delay:
134.17ps (force) RC delay: 32.84ps      lds: 15 pcap: 101.81ff  cap:
312.41ff (ext)  m2len: 0.00  m3len: 1125.00  m4len: 735.00
        hc1/u202/u242/u100/u3  (xbxor2df16s 16S)      Iport: D1_AD0PH
Oport: Q_AD0PF  IntDel: 167.60  net: hc1/u202/u242/cmp<3>    swg: df delay:
```

```
18.31ps (force)  RC delay: 0.11ps          lds: 1  pcap: 6.04ff     cap:
18.34ff (ext)  m2len: 8.00  m3len: 99.00  m4len: 0.00
        hc1/u202/u242/u110/u0    (xborff8df4s 4S)                    Iport:
D4_A0PF  IntDel: 273.10
        Time through Path: 928.23
```

From: Buffalo Chip [chip@rhea]
Sent: Monday, December 12, 1994 3:58 PM
To: 'geert@rhea'
Subject: pager log message

page from chip to geert:
Release euterpe/verilog/bsrc/ife BOM 38.0 initiated by hopper completed @ Mon Dec 12
13:53:57 PST 1994 with exit status 0.. chip

Hi,

 Here is a list of mux-ff paths taht cou;d be replaced by a single muxff cell. This will
save area, power and routing congestion. Please look at your blocks and see if it makes
sense to do the substitution.

                              Geert

iq/UpredGoMx1Q10/u0 (xbmux2dh2s) -> iq/UpredGoQ9/u0 (xbffdf2s) iq/UvldMx1Q10/u0
(xbmux2dh2s) -> iq/UvldQ9/u0 (xbffdf4s) iq/UpredGoMx2Q10/u0 (xbmux2dh2s) ->
iq/UpredGoQ9/u1 (xbffdf2s) iq/UvldMx2Q10/u0 (xbmux2dh2s) -> iq/UvldQ9/u1 (xbffdf2s)
iq/UpredGoMx3Q10/u0 (xbmux2dh2s) -> iq/UpredGoQ9/u2 (xbffdf4s) iq/UvldMx3Q10/u0
(xbmux2dh2s) -> iq/UvldQ9/u2 (xbffdf2s) iq/UvldMx3Q5/u0 (xbmux3dh2s) -> iq/UvldQ4/u3
(xbffdf2s) iq/UvldMx2Q5/u0 (xbmux3dh2s) -> iq/UvldQ4/u2 (xbffdf2s) iq/UvldMx1Q5/u0
(xbmux3dh2s) -> iq/UvldQS/u0 (xbffdf2s) iq/UvldMx0Q5/u0 (xbmux2dh2s) -> iq/UvldQ4/u0
(xbffdf2s) iq/UpredGoMx0Q5/u0 (xbmux2dh2s) -> iq/UpredGoQ4/u0 (xbffdf4s)
iq/UpredGoMx1Q5/u0 (xbmux3dh2s) -> iq/UpredGoQ4/u1 (xbffdf4s) iq/UpredGoMx2Q5/u0
(xbmux3dh2s) -> iq/UpredGoQ4/u2 (xbffdf2s) iq/UpredGoMx3Q5/u0 (xbmux3dh2s) ->
iq/UpredGoQ4/u3 (xbffdf4s)
iq/Uhxlt31MxQ10/u15 (xbmux2dh2s) -> iq/UhxltQ9/u95 (xbffdh2s)
iq/Uhxlt31MxQ10/u14 (xbmux2dh2s) -> iq/UhxltQ9/u94 (xbffdh2s)
iq/Uhxlt31MxQ10/u13 (xbmux2dh2s) -> iq/UhxltQ9/u93 (xbffdh2s)
iq/Uhxlt31MxQ10/u12 (xbmux2dh2s) -> iq/UhxltQ9/u92 (xbffdh2s)
iq/Uhxlt31MxQ10/u11 (xbmux2dh2s) -> iq/UhxltQ9/u91 (xbffdh2s) iq/Uhxlt31MxQ10/u10
(xbmux2dh2s) -> iq/UhxltQ9/u90 (xbffdh2s)
iq/Uhxlt31MxQ10/u9 (xbmux2dh2s) -> iq/UhxltQ9/u89 (xbffdh2s)
iq/Uhxlt31MxQ10/u8 (xbmux2dh2s) -> iq/UhxltQ9/u88 (xbffdh2s)
iq/Uhxlt31MxQ10/u7 (xbmux2dh2s) -> iq/UhxltQ9/u87 (xbffdh2s)
iq/Uhxlt31MxQ10/u6 (xbmux2dh2s) -> iq/UhxltQ9/u86 (xbffdh2s)
iq/Uhxlt31MxQ10/u5 (xbmux2dh2s) -> iq/UhxltQ9/u85 (xbffdh2s)
iq/Uhxlt31MxQ10/u4 (xbmux2dh2s) -> iq/UhxltQ9/u84 (xbffdh2s)
iq/Uhxlt31MxQ10/u3 (xbmux2dh2s) -> iq/UhxltQ9/u83 (xbffdh2s)
iq/Uhxlt31MxQ10/u2 (xbmux2dh2s) -> iq/UhxltQ9/u82 (xbffdh2s)
iq/Uhxlt31MxQ10/u1 (xbmux2dh2s) -> iq/UhxltQ9/u81 (xbffdh2s) iq/Uhxlt31MxQ10/u0
(xbmux2dh2s) -> iq/UhxltQ9/u80 (xbffdh2s)
iq/Uhxlt15MxQ10/u15 (xbmux2dh2s) -> iq/UhxltQ9/u79 (xbffdh2s)
iq/Uhxlt15MxQ10/u14 (xbmux2dh2s) -> iq/UhxltQ9/u78 (xbffdh2s)
iq/Uhxlt15MxQ10/u13 (xbmux2dh2s) -> iq/UhxltQ9/u77 (xbffdh2s)
iq/Uhxlt15MxQ10/u12 (xbmux2dh2s) -> iq/UhxltQ9/u76 (xbffdh2s)
iq/Uhxlt15MxQ10/u11 (xbmux2dh2s) -> iq/UhxltQ9/u75 (xbffdh2s) iq/Uhxlt15MxQ10/u10
(xbmux2dh2s) -> iq/UhxltQ9/u74 (xbffdh2s)
iq/Uhxlt15MxQ10/u9 (xbmux2dh2s) -> iq/UhxltQ9/u73 (xbffdh2s)
iq/Uhxlt15MxQ10/u8 (xbmux2dh2s) -> iq/UhxltQ9/u72 (xbffdh2s)
iq/Uhxlt15MxQ10/u7 (xbmux2dh2s) -> iq/UhxltQ9/u71 (xbffdh2s)
iq/Uhxlt15MxQ10/u6 (xbmux2dh2s) -> iq/UhxltQ9/u70 (xbffdh2s)
iq/Uhxlt15MxQ10/u5 (xbmux2dh2s) -> iq/UhxltQ9/u69 (xbffdh2s)
iq/Uhxlt15MxQ10/u4 (xbmux2dh2s) -> iq/UhxltQ9/u68 (xbffdh2s)
iq/Uhxlt15MxQ10/u3 (xbmux2dh2s) -> iq/UhxltQ9/u67 (xbffdh2s)
iq/Uhxlt15MxQ10/u2 (xbmux2dh2s) -> iq/UhxltQ9/u66 (xbffdh2s)
iq/Uhxlt15MxQ10/u1 (xbmux2dh2s) -> iq/UhxltQ9/u65 (xbffdh2s) iq/Uhxlt15MxQ10/u0
(xbmux2dh2s) -> iq/UhxltQ9/u64 (xbffdh2s)
iq/Uhxlt95MxQ10/u15 (xbmux2dh2s) -> iq/UhxltQ9/u63 (xbffdh2s)
iq/Uhxlt95MxQ10/u14 (xbmux2dh2s) -> iq/UhxltQ9/u62 (xbffdh2s)
iq/Uhxlt95MxQ10/u14 (xbmux2dh2s) -> iq/UhxltQ9/u62 (xbffdh2s)
iq/Uhxlt95MxQ10/u13 (xbmux2dh2s) -> iq/UhxltQ9/u61 (xbffdh2s)

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iq/Uhxlt95MxQ10/u12 (xbmux2dh2s) -> iq/UhxltQ9/u60 (xbffdh2s)
iq/Uhxlt95MxQ10/u11 (xbmux2dh2s) -> iq/UhxltQ9/u59 (xbffdh2s) iq/Uhxlt95MxQ10/u10
(xbmux2dh2s) -> iq/UhxltQ9/u58 (xbffdh2s)
iq/Uhxlt95MxQ10/u9 (xbmux2dh2s) -> iq/UhxltQ9/u57 (xbffdh2s)
iq/Uhxlt95MxQ10/u8 (xbmux2dh2s) -> iq/UhxltQ9/u56 (xbffdh2s)
iq/Uhxlt95MxQ10/u7 (xbmux2dh2s) -> iq/UhxltQ9/u55 (xbffdh2s)
iq/Uhxlt95MxQ10/u6 (xbmux2dh2s) -> iq/UhxltQ9/u54 (xbffdh2s)
iq/Uhxlt95MxQ10/u5 (xbmux2dh2s) -> iq/UhxltQ9/u53 (xbffdh2s)
iq/Uhxlt95MxQ10/u4 (xbmux2dh2s) -> iq/UhxltQ9/u52 (xbffdh2s)
iq/Uhxlt95MxQ10/u3 (xbmux2dh2s) -> iq/UhxltQ9/u51 (xbffdh2s)
iq/Uhxlt95MxMxQ10/u2 (xbmux2dh2s) -> iq/UhxltQ9/u50 (xbffdh2s)
iq/Uhxlt95MxQ10/u1 (xbmux2dh2s) -> iq/UhxltQ9/u49 (xbffdh2s) iq/Uhxlt95MxQ10/u0
(xbmux2dh2s) -> iq/UhxltQ9/u48 (xbffdh2s)
iq/Uhxlt79MxQ10/u15 (xbmux2dh2s) -> iq/UhxltQ9/u47 (xbffdh2s)
iq/Uhxlt79MxQ10/u14 (xbmux2dh2s) -> iq/UhxltQ9/u46 (xbffdh2s)
iq/Uhxlt79MxQ10/u13 (xbmux2dh2s) -> iq/UhxltQ9/u45 (xbffdh2s)
iq/Uhxlt79MxQ10/u12 (xbmux2dh2s) -> iq/UhxltQ9/u44 (xbffdh2s)
iq/Uhxlt79MxQ10/u11 (xbmux2dh2s) -> iq/UhxltQ9/u43 (xbffdh2s) iq/Uhxlt79MxQ10/u10
(xbmux2dh2s) -> iq/UhxltQ9/u42 (xbffdh2s)
iq/Uhxlt79MxQ10/u9 (xbmux2dh2s) -> iq/UhxltQ9/u41 (xbffdh2s)
iq/Uhxlt79MxQ10/u8 (xbmux2dh2s) -> iq/UhxltQ9/u40 (xbffdh2s)
iq/Uhxlt799MxQ10/u7 (xbmux2dh2s) -> iq/UhxltQ9/u39 (xbffdh2s)
iq/Uhxlt79MxQ10/u6 (xbmux2dh2s) -> iq/UhxltQ9/u38 (xbffdh2s)
iq/Uhxlt79MxQ10/u5 (xbmux2dh2s) -> iq/UhxltQ9/u37 (xbffdh2s)
iq/Uhxlt79MxQ10/u4 (xbmux2dh2s) -> iq/UhxltQ9/u36 (xbffdh2s)
iq/Uhxlt79MxQ10/u3 (xbmux2dh2s) -> iq/UhxltQ9/u35 (xbffdh2s)
iq/Uhxlt79MxQ10/u2 (xbmux2dh2s) -> iq/UhxltQ9/u34 (xbffdh2s)
iq/Uhxlt79MxQ10/u1 (xbmux2dh2s) -> iq/UhxltQ9/u33 (xbffdh2s) iq/Uhxlt79MxQ10/u0
(xbmux2dh2s) -> iq/UhxltQ9/u32 (xbffdh2s)
iq/Uhxlt63MxQ10/u15 (xbmux2dh2s) -> iq/UhxltQ9/u31 (xbffdh2s)
iq/Uhxlt63MxQ10/u14 (xbmux2dh2s) -> iq/UhxltQ9/u30 (xbffdh2s)
iq/Uhxlt63MxQ10/u13 (xbmux2dh2s) -> iq/UhxltQ9/u29 (xbffdh2s)
iq/Uhxlt63MxQ10/u12 (xbmux2dh2s) -> iq/UhxltQ9/u28 (xbffdh2s)
iq/Uhxlt63MxQ10/u11 (xbmux2dh2s) -> iq/UhxltQ9/u27 (xbffdh2s) iq/Uhxlt63MxQ10/u10
(xbmux2dh2s) -> iq/UhxltQ9/u26 (xbffdh2s)
iq/Uhxlt63MxQ10/u9 (xbmux2dh2s) -> iq/UhxltQ9/u25 (xbffdh2s)
iq/Uhxlt63MxQ10/u8 (xbmux2dh2s) -> iq/UhxltQ9/u24 (xbffdh2s)
iq/Uhxlt63MxQ10/u7 (xbmux2dh2s) -> iq/UhxltQ9/u23 (xbffdh2s)
iq/Uhxlt63MxQ10/u6 (xbmux2dh2s) -> iq/UhxltQ9/u22 (xbffdh2s)
iq/Uhxlt63MxQ10/u5 (xbmux2dh2s) -> iq/UhxltQ9/u21 (xbffdh2s)
iq/Uhxlt63MxQ10/u4 (xbmux2dh2s) -> iq/UhxltQ9/u20 (xbffdh2s)
iq/Uhxlt63MxQ10/u3 (xbmux2dh2s) -> iq/UhxltQ9/u19 (xbffdh2s)
iq/Uhxlt63MxQ10/u2 (xbmux2dh2s) -> iq/UhxltQ9/u18 (xbffdh2s)
iq/Uhxlt63MxQ10/u1 (xbmux2dh2s) -> iq/UhxltQ9/u17 (xbffdh2s) iq/Uhxlt63MxQ10/u0
(xbmux2dh2s) -> iq/UhxltQ9/u16 (xbffdh2s)
iq/Uhxlt47MxQ10/u15 (xbmux2dh2s) -> iq/UhxltQ9/u15 (xbffdh2s)
iq/Uhxlt47MMxQ10/u14 (xbmux2dh2s) -> iq/UhxltQ9/u14 (xbffdh2s)
iq/Uhxlt47MxQ10/u13 (xbmux2dh2s) -> iq/UhxltQ9/u13 (xbffdh2s)
iq/Uhxlt47MxQ10/u12 (xbmux2dh2s) -> iq/UhxltQ9/u12 (xbffdh2s)
iq/Uhxlt47MxQ10/u11 (xbmux2dh2s) -> iq/UhxltQ9/u11 (xbffdh2s) iq/Uhxlt47MxQ10/u10
(xbmux2dh2s) -> iq/UhxltQ9/u10 (xbffdh2s)
iq/Uhxlt47MxQ10/u9 (xbmux2dh2s) -> iq/UhxltQ9/u9 (xbffdh2s)
iq/Uhxlt47MxQ10/u8 (xbmux2dh2s) -> iq/UhxltQ9/u8 (xbffdh2s)
iq/Uhxlt47MxQ10/u7 (xbmux2dh2s) -> iq/UhxltQ9/u7 (xbffdh2s)
iq/Uhxlt47MxQ10/u6 (xbmux2dh2s) -> iq/UhxltQ9/u6 (xbffdh2s)
iq/Uhxlt47MxQ10/u5 (xbmux2dh2s) -> iq/UhxltQ9/u5 (xbffdh2s)
iq/Uhxlt47MxQ10/u4 (xbmux2dh2s) -> iq/UhxltQ9/u4 (xbffdh2s)
iq/Uhxlt47MxQ10/u3 (xbmux2dh2s) -> iq/UhxltQ9/u3 (xbffdh2s)
iq/Uhxlt47MxQ10/u2 (xbmux2dh2s) -> iq/UhxltQ9/u2 (xbffdh2s) iq/Uhxlt47MxQ10/u0
(xbmux2dh2s) -> iq/UhxltQ9/u0 (xbffdh2s)
iq/Uhxlt127MxQ5/u15 (xbmux3dh2s) -> iq/UhxltQ4/u127 (xbffdh2s)
iq/Uhxlt127MxQ5/u14 (xbmux3dh2s) -> iq/UhxltQ4/u126 (xbffdh2s)
iq/Uhxlt127MxQ5/u13 (xbmux3dh2s) -> iq/UhxltQ4/u125 (xbffdh2s)
iq/Uhxlt127MxQ5/u12 (xbmux3dh2s) -> iq/UhxltQ4/u124 (xbffdh2s)
iq/Uhxlt127MxQ5/u11 (xbmux3dh2s) -> iq/UhxltQ4/u123 (xbffdh2s) iq/Uhxlt127MxQ5/u10
(xbmux3dh2s) -> iq/UhxltQ4/u122 (xbffdh2s)
iq/Uhxlt127MxQ5/u9 (xbmux3dh2s) -> iq/UhxltQ4/u121 (xbffdh2s)
iq/Uhxlt127MxQ5/u8 (xbmux3dh2s) -> iq/UhxltQ4/u120 (xbffdh2s)
```

```
iq/Uhxlt127MxQ5/u7 (xbmux3dh2s) -> iq/UhxltQ4/u119 (xbffdh2s)
iq/Uhxlt127MxQ5/u6 (xbmux3dh2s) -> iq/UhxltQ4/u118 (xbffdh2s)
iq/Uhxlt127MxQ5/u5 (xbmux3dh2s) -> iq/UhxltQ4/u117 (xbffdh2s)
iq/Uhxlt127MxQ5/u4 (xbmux3dh2s) -> iq/UhxltQ4/u116 (xbffdh2s)
iq/Uhxlt127MxQ5/u3 (xbmux3dh2s) -> iq/UhxltQ4/u115 (xbffdh2s)
iq/Uhxlt127MxQ5/u2 (xbmux3dh2s) -> iq/UhxltQ4/u114 (xbffdh2s)
iq/Uhxlt127MxQ5/u1 (xbmux3dh2s) -> iq/UhxltQ4/u113 (xbffdh2s) iq/Uhxlt127MxQ5/u0
(xbmux3dh2s) -> iq/UhxltQ4/u112 (xbffdh2s)
iq/Uhxlt111MxQ5/u15 (xbmux3dh2s) -> iq/UhxltQ4/u111 (xbffdh2s)
iq/Uhxlt111MxQ5/u14 (xbmux3dh2s) -> iq/UhxltQ4/u110 (xbffdh2s)
iq/Uhxlt111MxQ5/u13 (xbmux3dh2s) -> iq/UhxltQ4/u109 (xbffdh2s)
iq/Uhxlt111MxQ5/u12 (xbmux3dh2s) -> iq/UhxltQ4/u108 (xbffdh2s)
iq/Uhxlt111MxQ5/u11 (xbmux3dh2s) -> iq/UhxltQ4/u107 (xbffdh2s) iq/Uhxlt111MxQ5/u10
(xbmux3dh2s) -> iq/UhxltQ4/u106 (xbffdh2s)
iq/Uhxlt111MxQ5/u9 (xbmux3dh2s) -> iq/UhxltQ4/u105 (xbffdh2s)
iq/Uhxlt111MxQ5/u8 (xbmux3dh2s) -> iq/UhxltQ4/u104 (xbffdh2s)
iq/Uhxlt111MxQ5/u7 (xbmux3dh2s) -> iq/UhxltQ4/u103 (xbffdh2s)
iq/Uhxlt111MxQ5/u6 (xbmux3dh2s) -> iq/UhxltQ4/u102 (xbffdh2s)
iq/Uhxlt111MxQ5/u5 (xbmux3dh2s) -> iq/UhxltQ4/u101 (xbffdh2s)
iq/Uhxlt111MxQ5/u4 (xbmux3dh2s) -> iq/UhxltQ4/u100 (xbffdh2s)
iq/Uhxlt111MxQ5/u3 (xbmux3dh2s) -> iq/UhxltQ4/u99 (xbffdh2s)
iq/Uhxlt111MxQ5/u2 (xbmux3dh2s) -> iq/UhxltQ4/u98 (xbffdh2s)
iq/Uhxlt111MxQ5/u1 (xbmux3dh2s) -> iq/UhxltQ4/u97 (xbffdh2s) iq/Uhxlt1111MxQ5/u0
(xbmux3dh2s) -> iq/UhxltQ4/u96 (xbffdh2s)
iq/Uhxlt95MxQ5/u15 (xbmux3dh2s) -> iq/UhxltQ4/u95 (xbffdh2s)
iq/Uhxlt95MxQ5/u14 (xbmux3dh2s) -> iq/UhxltQ4/u94 (xbffdh2s)
iq/Uhxlt95MxQ5/u13 (xbmux3dh2s) -> iq/UhxltQ4/u93 (xbffdh2s)
iq/Uhxlt95MxQ5/u12 (xbmux3dh2s) -> iq/UhxltQ4/u92 (xbffdh2s)
iq/Uhxlt95MxQ5/u11 (xbmux3dh2s) -> iq/UhxltQ4/u91 (xbffdh2s) iq/Uhxlt95MxQ5/u10
(xbmux3dh2s) -> iq/UhxltQ4/u90 (xbffdh2s)
iq/Uhxlt95MxQ5/u9 (xbmux3dh2s) -> iq/UhxltQ4/u89 (xbffdh2s)
iq/Uhxlt95MxQ5/u8 (xbmux3dh2s) -> iq/UhxltQ4/u88 (xbffdh2s)
iq/Uhxlt95MxQ5/u7 (xbmux3dh2s) -> iq/UhxltQ4/u87 (xbffdh2s)
iq/Uhxlt95MxQ5/u6 (xbmux3dh2s) -> iq/UhxltQ4/u86 (xbffdh2s)
iq/Uhxlt95MxQ5/u5 (xbmux3dh2s) -> iq/UhxltQ4/u85 (xbffdh2s)
iq/Uhxlt95MxQ5/u4 (xbmux3dh2s) -> iq/UhxltQ4/u84 (xbffdh2s)
iq/Uhxlt95MxQ5/u3 (xbmux3dh2s) -> iq/UhxltQ4/u83 (xbffdh2s)
iq/Uhxlt95MxQ5/u2 (xbmux3dh2s) -> iq/UhxltQ4/u82 (xbffdh2s)
iq/Uhxlt95MxQ5/u1 (xbmux3dh2s) -> iq/UhxltQ4/u81 (xbffdh2s) iq/Uhxlt95MxQ5/u0 (xbmux3dh2s)
-> iq/UhxltQ4/u80 (xbffdh2s)
iq/Uhxlt79MxQ5/u15 (xbmux3dh2s) -> iq/UhxltQ4/u79 (xbffdh2s)
iq/Uhxlt79MxQ5/u14 (xbmux3dh2s) -> iq/UhxltQ4/u78 (xbffdh2s)
iq/Uhxlt79MxQ5/u13 (xbmux3dh2s) -> iq/UhxltQ4/u77 (xbffdh2s)
iq/Uhxlt79MxQ5/u12 (xbmux3dh2s) -> iq/UhxltQ4/u76 (xbffdh2s)
iq/Uhxlt79MxQ5/u11 (xbmux3dh2s) -> iq/UhxltQ4/u75 (xbffdh2s) iq/Uhxlt79MxQ5/u10
(xbmux3dh2s) -> iq/UhxltQ4/u74 (xbffdh2s)
iq/Uhxlt79MxQ5/u9 (xbmux3dh2s) -> iq/UhxltQ4/u73 (xbffdh2s)
iq/Uhxlt79MxQ5/u8 (xbmux3dh2s) -> iq/UhxltQ4/u72 (xbffdh2s)
iq/Uhxlt79MxQ5/u7 (xbmux3dh2s) -> iq/UhxltQ4/u71 (xbffdh2s)
iq/Uhxlt79MxQ5/u6 (xbmux3dh2s) -> iq/UhxltQ4/u70 (xbffdh2s)
iq/Uhxlt79MxQ5/u5 (xbmux3dh2s) -> iq/UhxltQ4/u69 (xbffdh2s)
iq/Uhxlt79MxQ5/u4 (xbmux3dh2s) -> iq/UhxltQ4/u68 (xbffdh2s)
iq/Uhxlt79MxQ5/u3 (xbmux3dh2s) -> iq/UhxltQ4/u67 (xbffdh2s)
iq/Uhxlt79MxQ5/u2 (xbmux3dh2s) -> iq/UhxltQ4/u66 (xbffdh2s)
iq/Uhxlt79MxQ5/u1 (xbmux3dh2s) -> iq/UhxltQ4/u65 (xbffdh2s) iq/Uhxlt79MxQ5/u0 (xbmux3dh2s)
-> iq/UhxltQ4/u64 (xbffdh2s)
iq/Uhxlt63MxQ5/u15 (xbmux3dh2s) -> iq/UhxltQ4/u63 (xbffdh2s)
iq/Uhxlt63MxQ5/u14 (xbmux3dh2s) -> iq/UhxltQ4/u62 (xbffdh2s)
iq/Uhxlt63MxQ5/u13 (xbmux3dh2s) -> iq/UhxltQ4/u61 (xbffdh2s)
iq/Uhxlt63MxQ5/u12 (xbmux3dh2s) -> iq/UhxltQ4/u60 (xbffdh2s)
iq/Uhxlt63MxQ5/u11 (xbmux3dh2s) -> iq/UhxltQ4/u59 (xbffdh2s) iq/Uhxlt63MxQ5/u10
(xbmux3dh2s) -> iq/UhxltQ4/u58 (xbffdh2s)
iq/Uhxlt63MxQ5/u9 (xbmux3dh2s) -> iq/UhxltQ4/u57 (xbffdh2s)
iq/Uhxlt63MxQ5/u8 (xbmux3dh2s) -> iq/UhxltQ4/u56 (xbffdh2s)
iq/Uhxlt63MxQ5/u7 (xbmux3dh2s) -> iq/UhxltQ4/u55 (xbffdh2s)
iq/Uhxlt63MxQ5/u6 (xbmux3dh2s) -> iq/UhxltQ4/u54 (xbffdh2s)
iq/Uhxlt63MxQ5/u5 (xbmux3dh2s) -> iq/UhxltQ4/u53 (xbffdh2s)
iq/Uhxlt63MxQ5/u4 (xbmux3dh2s) -> iq/UhxltQ4/u52 (xbffdh2s)
```

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iq/Uhxlt63MxQ5/u3 (xbmux3dh2s) -> iq/UhxltQ4/u51 (xbffdh2s)
iq/Uhxlt63MxQ5/u2 (xbmux3dh2s) -> iq/UhxltQ4/u50 (xbffdh2s)
iq/Uhxlt63MxQ5/u1 (xbmux3dh2s) -> iq/UhxltQ4/u49 (xbffdh2s) iq/Uhxlt63MxQ5/u0 (xbmux3dh2s)
-> iq/UhxltQ4/u48 (xbffdh2s)
iq/Uhxlt47MxQ5/u15 (xbmux3dh2s) -> iq/UhxltQ4/u47 (xbffdh2s)
iq/Uhxlt47MxQ5/u14 (xbmux3dh2s) -> iq/UhxltQ4/u46 (xbffdh2s)
iq/Uhxlt47MxQ5/u13 (xbmux3dh2s) -> iq/UhxltQ4/u45 (xbffdh2s)
iq/Uhxlt47MxQQ5/u12 (xbmux3dh2s) -> iq/UhxltQ4/u44 (xbffdh2s)
iq/Uhxlt47MxQ5/u11 (xbmux3dh2s) -> iq/UhxltQ4/u43 (xbffdh2s) iq/Uhxlt47MxQ5/u10
(xbmux3dh2s) -> iq/UhxltQ4/u42 (xbffdh2s)
iq/Uhxlt47MxQ5/u9 (xbmux3dh2s) -> iq/UhxltQ4/u41 (xbffdh2s)
iq/Uhxlt47MxQ5/u8 (xbmux3dh2s) -> iq/UhxltQ4/u40 (xbffdh2s)
iq/Uhxlt47MxQ5/u7 (xbmux3dh2s) -> iq/UhxltQ4/u39 (xbffdh2s)
iq/Uhxlt47MxQ5/u6 (xbmux3dh2s) -> iq/UhxltQ4/u38 (xbffdh2s)
iq/Uhxlt47MxQ5/u5 (xbmux3dh2s) -> iq/UhxltQ4/u37 (xbffdh2s)
iq/Uhxlt47MxQ5/u4 (xbmux3dh2s) -> iq/UhxltQ4/u36 (xbffdh2s)
iq/Uhxlt47MxQ5/u3 (xbmux3dh2s) -> iq/UhxltQ4/u35 (xbffdh2s)
iq/Uhxlt47MxQ5/u2 (xbmux3dh2s) -> iq/UhxltQ4/u34 (xbffdh2s)
iq/Uhxlt47MxQ5/u1 (xbmux3dh2s) -> iq/UhxltQ4/u33 (xbffdh2s) iq/Uhxlt47MxQ5/u0 (xbmux3dh2s)
-> iq/UhxltQ4/u32 (xbffdh2s)
iq/UinstHQR/u15 (xbmux8dh3s) -> iq/UinstQS/u31 (xbffdh24s)
iq/Uhxlt31MxQ5/u15 (xbmux2dh2s) -> iq/UhxltQ4/u31 (xbffdh2s)
iq/UinstHQR/u14 (xbmux8dh3s) -> iq/UinstQS/u30 (xbffdh24s)
iq/Uhxlt31MxQ5/u14 (xbmux2dh2s) -> iq/UhxltQ4/u30 (xbffdh2s)
iq/UinstHQR/u13 (xbmux8dh3s) -> iq/UinstQS/u29 (xbffdh24s)
iq/Uhxlt31MxQ5/u13 (xbmux2dh2s) -> iq/UhxltQ4/u29 (xbffdh2s)
iq/UinstHQR/u12 (xbmux8dh3s) -> iq/UinstQS/u28 (xbffdh24s)
iq/Uhxlt31MxQ5/u12 (xbmux2dh2s) -> iq/UhxltQ4/u28 (xbffdh2s)
iq/UinstHQR/u11 (xbmux8dh3s) -> iq/UinstQS/u27 (xbffdh24s)
iq/Uhxlt31MxQ5/u11 (xbmux2dh2s) -> iq/UhxltQ4/u27 (xbffdh2s) iq/UinstHQR/u10 (xbmux8dh3s)
-> iq/UinstQS/u26 (xbffdh24s) iq/Uhxlt31MxQ5/u10 (xbmux2dh2s) -> iq/UhxltQ4/u26 (xbffdh2s)
iq/UinstHQR/u9 (xbmux8dh3s) -> iq/UinstQS/u25 (xbffdh24s)
iq/Uhxlt31MxQ5/u9 (xbmux2dh2s) -> iq/UhxltQ4/u25 (xbffdh2s)
iq/UinstHQR/u8 (xbmux8dh3s) -> iq/UinstQS/u24 (xbffdh24s)
iq/Uhxlt31MxQ5/u8 (xbmux2dh2s) -> iq/UhxltQ4/u24 (xbffdh2s)
iq/UinstHQR/u7 (xbmux8dh3s) -> iq/UinstQS/u23 (xbffdh24s)
iq/Uhxlt31MxQ5/u7 (xbmux2dh2s) -> iq/UhxltQ4/u23 (xbffdh2s)
iq/UinstHQR/u6 (xbmux8dh3s) -> iq/UinstQS/u22 (xbffdh24s)
iq/Uhxlt31MxQ5/u6 (xbmux2dh2s) -> iq/UhxltQ4/u22 (xbffdh2s)
iq/UinstHQR/u5 (xbmux8dh3s) -> iq/UinstQS/u21 (xbffdh24s)
iq/Uhxlt31MxQ5/u5 (xbmux2dh2s) -> iq/UhxltQ4/u21 (xbffdh2s)
iq/UinstHQR/u4 (xbmux8dh3s) -> iq/UinstQS/u20 (xbffdh24s)
iq/Uhxlt31MxQ5/u4 (xbmux2dh2s) -> iq/UhxltQ4/u20 (xbffdh2s)
iq/UinstHQR/u3 (xbmux8dh3s) -> iq/UinstQS/u19 (xbffdh24s)
iq/Uhxlt31MxQ5/u3 (xbmux2dh2s) -> iq/UhxltQ4/u19 (xbffdh2s)
iq/UinstHQR/u2 (xbmux8dh3s) -> iq/UinstQS/u18 (xbffdh24s)
iq/Uhxlt31MxQ5/u2 (xbmux2dh2s) -> iq/UhxltQ4/u18 (xbffdh2s)
iq/UinstHQR/u1 (xbmux8dh3s) -> iq/UinstQS/u17 (xbffdh24s)
iq/Uhxlt31MxQ5/u1 (xbmux2dh2s) -> iq/UhxltQ4/u17 (xbffdh2s) iq/UinstHQR/u0 (xbmux8dh3s) ->
iq/UinstQS/u16 (xbffdh24s) iq/Uhxlt31MxQ5/u0 (xbmux2dh2s) -> iq/UhxltQ4/u16 (xbffdh2s)
iq/UinstLQR/u15 (xbmux8dh3s) -> iq/UinstQS/u15 (xbffdh24s)
iq/Uhxlt15MxQ5/u15 (xbmux2dh2s) -> iq/UhxltQ4/u15 (xbffdh2s)
iq/UinstLQR/u14 (xbmux8dh3s) -> iq/UinstQS/u14 (xbffdh24s)
iq/Uhxlt15MxQ5/u14 (xbmux2dh2s) -> iq/UhxltQ4/u14 (xbffdh2s)
iq/UinstLQR/u13 (xbmux8dh3s) -> iq/UinstQS/u13 (xbffdh24s)
iq/Uhxlt15MxQ5/u13 (xbmux2dh2s) -> iq/UhxltQ4/u13 (xbffdh2s)
iq/UinstLQR/u12 (xbmux8dh3s) -> iq/UinstQS/u12 (xbffdh24s)
iq/Uhxlt15MxQ5/u12 (xbmux2dh2s) -> iq/UhxltQ4/u12 (xbffdh2s)
iq/UinstLQR/u11 (xbmux8dh3s) -> iq/UinstQS/u11 (xbffdh24s)
iq/Uhxlt15MxQ5/u11 (xbmux2dh2s) -> iq/UhxltQ4/u11 (xbffdh2s) iq/UinstLQR/u10 (xbmux8dh3s)
-> iq/UinstQS/u10 (xbffdh24s) iq/Uhxlt15MxQ5/u10 (xbmux2dh2s) -> iq/UhxltQ4/u10 (xbffdh2s)
iq/UinstLQR/u9 (xbmux8dh3s) -> iq/UinstQS/u9 (xbffdh24s)
iq/Uhxlt15MxQ5/u9 (xbmux2dh2s) -> iq/UhxltQ4/u9 (xbffdh2s)
iq/UinstLQR/u8 (xbmux8dh3s) -> iq/UinstQS/u8 (xbffdh24s)
iq/Uhxlt15MxQ5/u8 (xbmux2dh2s) -> iq/UhxltQ4/u8 (xbffdh2s)
iq/UinstLQR/u7 (xbmux8dh3s) -> iq/UinstQS/u7 (xbffdh24s)
iq/Uhxlt15MxQ5/u7 (xbmux2dh2s) -> iq/UhxltQ4/u7 (xbffdh2s)
iq/UinstLQR/u6 (xbmux8dh3s) -> iq/UinstQS/u6 (xbffdh24s)
```

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iq/Uhxlt15MxQ5/u6 (xbmux2dh2s) -> iq/UhxltQ4/u6 (xbffdh2s)
iq/UinstLQR/u5 (xbmux8dh3s) -> iq/UinstQS/u5 (xbffdh24s)
iq/Uhxlt15MxQ5/u5 (xbmux2dh2s) -> iq/UhxltQ4/u5 (xbffdh2s)
iq/UinstLQR/u4 (xbmux8dh3s) -> iq/UinstQS/u4 (xbffdh24s)
iq/Uhxlt15MxQ5/u4 (xbmux2dh2s) -> iq/UhxltQ4/u4 (xbffdh2s)
iq/UinstLQR/u3 (xbmux8dh3s) -> iq/UinstQS/u3 (xbffdh24s)
iq/Uhxlt15MxQ5/u3 (xbmux2dh2s) -> iq/UhxltQ4/u3 (xbffdh2s)
iq/UinstLQR/u2 (xbmux8dh3s) -> iq/UinstQS/u2 (xbffdh24s)
iq/Uhxlt15MxQ5/u2 (xbmux2dh2s) -> iq/UhxltQ4/u2 (xbffdh2s)
iq/UinstLQR/u1 (xbmux8dh3s) -> iq/UinstQS/u1 (xbffdh24s)
iq/Uhxlt15MxQ5/u1 (xbmux2dh2s) -> iq/UhxltQ4/u1 (xbffdh2s) iq/UinstLQR/u0 (xbmux8dh3s) ->
iq/UinstQS/u0 (xbffdh24s) iq/Uhxlt15MxQ5/u0 (xbmux2dh2s) -> iq/UhxltQ4/u0 (xbffdh2s)
rgxmit/UvldIGoNCnclRR/u0 (xbmux2dh2s) -> rgxmit/UvldIncPcRR/u0 (xbffdh24s)
rg/rgcr/r4/UdstWStbHWNWM/u0 (xbmux2dh2s) -> rg/rgcr/r4/UdstWStbWN/u1
(xbffdh6s)
rg/rgcr/r3/UdstWStbHWNWM/u0 (xbmux2dh2s) -> rg/rgcr/r3/UdstWStbWN/u1
(xbffdh6s)
rg/rgcr/r2/UdstWStbHWNWM/u0 (xbmux2dh2s) -> rg/rgcr/r2/UdstWStbWN/u1
(xbffdh6s)
rg/rgcr/r1/UdstWStbHWNWM/u0 (xbmux2dh2s) -> rg/rgcr/r1/UdstWStbWN/u1
(xbffdh6s)
rg/rgcr/r0/UdstWStbHWNWM/u0 (xbmux2dh2s) -> rg/rgcr/r0/UdstWStbWN/u1
(xbffdh6s)
rg/rgcr/r4/UdstWStbLWNWM/u0 (xbmux2dh2s) -> rg/rgcr/r4/UdstWStbWN/u0
(xbffdh6s)
rg/rgcr/r3/UdstWStbLWNWM/u0 (xbmux2dh2s) -> rg/rgcr/r3/UdstWStbWN/u0
(xbffdh6s)
rg/rgcr/r2/UdstWStbLWNWM/u0 (xbmux2dh2s) -> rg/rgcr/r2/UdstWStbWN/u0
(xbffdh6s)
rg/rgcr/r1/UdstWStbLWNWM/u0 (xbmux2dh2s) -> rg/rgcr/r1/UdstWStbWN/u0
(xbffdh6s)
rg/rgcr/r0/UdstWStbLWNWM/u0 (xbmux2dh2s) -> rg/rgcr/r0/UdstWStbWN/u0
(xbffdh6s)
rg/rgpc/UpcPlOrZero63RQ/u31 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u63
(xbffdh2s)
rg/rgpc/UpcPlOrZero63RQ/u30 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u62
(xbffdh2s)
rg/rgpc/UpcPlOrZero63RQ/u29 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u61
(xbffdh2s)
rg/rgpc/UpcPlOrZero63RQ/u28 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u60
(xbffdh2s)
rg/rgpc/UpcPlOrZero63RQ/u27 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u59
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u26 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u58
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u25 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u57
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u24 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u56
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u23 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u55
(xbffdh2s)
rg/rgpc/UpcPlOrZero63RQ/u22 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u54
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u21 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u53
(xbffdh2s)
rg/rgpc/UpcPlOrZero63RQ/u20 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u52
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u19 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u51
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u18 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u50
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u17 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u49
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u16 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u48
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u15 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u47
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u14 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u46
```

(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u13 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u45
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u12 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u44
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u11 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u43
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u10 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u42
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u9 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u41
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u8 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u40
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u7 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u39 (xbffdh2s)`
rg/rgpc/UpcPlOrZero63RQ/u6 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u38
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u5 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u37
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u4 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u36
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u2 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u34
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u1 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u33
(xbffdh3s)
rg/rgpc/UpcPlOrZero63RQ/u0 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u32
(xbffdh3s)
rg/rgpc/UpcPlOrZero31RQ/u29 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u31
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u28 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u30
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u27 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u29
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u26 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u28
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u25 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u27
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u24 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u26
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u23 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u25
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u22 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u24
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u21 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u23
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u20 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u22
(xbffdh3s)
rg/rgpc/UpcPlOrZero31RQ/u19 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u21
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u18 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u20
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u17 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u19
(xbffbdh6s)
rg/rgpc/UpcPlOrZero31RQ/u16 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u18
(xbffdh3s)
rg/rgpc/UpcPlOrZero31RQ/u15 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u17
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u14 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u16
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u13 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u15
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u12 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u14
(xbffdh3s)
rg/rgpc/UpcPlOrZero31RQ/u11 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u13
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u10 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u12
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u9 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u11
(xbffdh3s)

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rg/rgpc/UpcPlOrZero31RQ/u8 (xbmux4dh3s) -> rg/rgpc/UpcPlOrZeroRR/u10
(xbffdh3s)
rg/rgpc/UpcPlOrZero31RQ/u7 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u9
(xbffdh3s)
rg/rgpc/UpcPlOrZero31RQ/u6 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u8
(xbffdh3s)
rg/rgpc/UpcPlOrZero31RQ/u5 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u7
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u4 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u6
(xbffdh2s)
rg/rgpc/UpcPlOrZero31RQ/u3 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u5
(xbffdh3s)
rg/rgpc/UpcPlOrZero31RQ/u2 (xbmux4dh3s) -> rg/rgpc/UpcPlOrZeroRR/u4
(xbffdh3s)
rg/rgpc/UpcPlOrZero31RQ/u1 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u3
(xbffdh3s)
rg/rgpc/UpcPlOrZero31RQ/u0 (xbmux4dh2s) -> rg/rgpc/UpcPlOrZeroRR/u2
(xbffdh3s)
mc/u02/u284a/u0 (xbmux2dh2s) -> mc/u02/xlu00/u0 (xbffdf8s) at/UatPaSel/UpaSel63/u0
(xbmux3dh2s) -> at/Upa6348R11/u15 (xbffbdf4s) at/UatPaSel/UpaSel62/u0 (xbmux3dh2s) ->
at/Upa6348R11/u14 (xbffdf4s) at/UatPaSel/UpaSel61/u0 (xbmux3dh2s) -> at/Upa6348R11/u13
(xbffdf4s) at/UatPaSel/UpaSel60/u0 (xbmux3dh2s) -> at/Upa6348R11/u12 (xbffdf4s)
at/UatPaSel/UpaSel59/u0 (xbmux3dh2s) -> at/Upa6348R11/u11 (xbffdf4s)
at/UatPaSel/UpaSel58/u0 (xbmux3dh2s) -> at/Upa6348R11/u10 (xbffdf4s)
at/UatPaSel/UpaSel57/u0 (xbmux3dh2s) -> at/Upa6348R11/u9 (xbffdf4s)
at/UatPaSel/UpaSel56/u0 (xbmux3dh2s) -> at/Upa6348R11/u8 (xbffdf4s)
at/UatPaSel/UpaSel55/u0 (xbmux3dh2s) -> at/Upa6348R11/u7 (xbffdf4s)
at/UatPaSel/UpaSel54/u0 (xbmux3dh2s) -> at/Upa6348R11/u6 (xbffdf4s)
at/UatPaSel/UpaSel53/u0 (xbmux3dh2s) -> at/Upa6348R11/u5 (xbffdf4s)
at/UatPaSel/UpaSel52/u0 (xbmux3dh2s) -> at/Upa6348R11/u4 (xbffdf4s)
at/UatPaSel/UpaSel51/u0 (xbmux3dh2s) -> at/Upa6348R11/u3 (xbffdf4s)
at/UatPaSel/UpaSel50/u0 (xbmux3dh2s) -> at/Upa6348R11/u2 (xbffdf4s)
at/UatPaSel/UpaSel49/u0 (xbmux3dh2s) -> at/Upa6348R11/u1 (xbffdf4s)
at/UatPaSel/UpaSel48/u0 (xbmux3dh2s) -> at/Upa6348R11/u0 (xbffdf4s)
at/UatPaSel/UpaSel44/u0 (xbmux3dh2s) -> at/Upa4700R11/u44 (xbffdf16s)
at/UatPaSel/UpaSel8/u0 (xbmux3dh3s) -> at/Upa4700R11/u8 (xbffdf6s) at/UatPaSel/UpaSel7/u0
(xbmux3dh2s) -> at/Upa4700R11/u7 (xbffdf6s) at/UatPaSel/UpaSel6/u0 (xbmux3dh2s) ->
at/Upa4700R11/u6 (xbffbdf6s)
```

From: lisar (Lisa Robinson)

Sent: Monday, December 12, 1994 4:48 PM

To: 'dickson'; 'jeffm'

Cc: 'tbr'; 'mws'

Subject: Yeah

test 1 has started to fab!

```
1029360: 0,000c 1,dc100fab 10,1,fcffffff 0000800000c0001b 00 1f,0,0000800000c000240000800000c00024 00000,0,1
 1029480: 4,0009 0,dc0c0000 01,0,dc0c0000 0000800000c0002f 00 02,0,0000800000c000240000800000c00024
00000,1,1
 1029600: 4,0009 1,dc100fab 02,0,fcffffff 0000800000c00027 00 01,1,0000000000000fab0000000000000fab 00000,0,1
 1029720: 0,0009 1,dc100fab 04,0,fcffffff 0000800000c0002b 01 1f,0,0000000000000000000000000000000000 00000,0,1
 1029840: 6,0009 1,dc100fab 08,1,fcffffff 0000800000c0002b 00 1f,0,0000800000c000240000800000c00024 00000,0,1
 1029960: 0,000c 1,fcffffff 10,1,dc100fab 0000800000c0001b 00 02,0,0000800000c000240000800000c00024 00000,1,1
 1030080: 4,0009 0,dc0c0000 01,0,dc0c0000 0000800000c00027 00 1f,1,0000000000000fab0000000000000fab 00000,1,1
 1030200: 0,0009 1,dc100fab 02,0,fcffffff 0000800000c0002b 00 01,0,0000800000c0002c0000800000c0002c 00000,0,1
 1030320: 6,0009 1,dc100fab 04,1,fcffffff 0000800000c0002b 00 1f,0,0000000000000000000000000000000000 00000,0,1
 1030440: 4,0009 1,fcffffff 08,1,dc100fab 0000800000c0002f 00 02,0,0000800000c000240000800000c00024 00000,1,1
 1030560: 0,000c 1,dc100fab 10,0,fcffffff 0000800000c0001b 00 1f,1,0000000000000fab0000000000000fab 00000,1,1
 1030680: 0,0009 0,dc0c0000 01,0,dc0c0000 0000800000c0002b 01 1f,0,0000800000c0002c0000800000c0002c 00000,0,1
 1030800: 6,0009 1,dc100fab 02,1,fcffffff 0000800000c0002b 00 01,0,0000800000c000240000800000c00024 00000,0,1
 1030920: 4,0009 1,fcffffff 04,1,dc100fab 0000800000c0002f 00 02,0,0000000000000000000000000000000000 00000,1,1
 1031040: 4,0009 1,dc100fab 08,0,fcffffff 0000800000c00027 00 1f,1,0000000000000fab0000000000000fab 00000,1,1
 1031160: 0,000c 1,dc100fab 10,0,fcffffff 0000800000c0001b 01 1f,0,0000800000c0002c0000800000c0002c 00000,0,1
 1031280: 6,0009 0,dc0c0000 01,0,dc0c0000 0000800000c0002b 00 1f,0,0000800000c000240000800000c00024
00000,0,1
 1031400: 4,0009 1,fcffffff 02,1,dc100fab 0000800000c0002f 00 01,0,0000800000c000240000800000c00024 00000,0,1
 1031520: 4,0009 1,dc100fab 04,0,fcffffff 0000800000c00027 00 1f,0,0000000000000000000000000000000000 0
```

haven't stashed it yet but it is on rhodan /s3/euterpe/verilog/bsrc

wrap.log verilog.dump.

Congrats. Rich.

Lisa R.

From:	tom (Tom Laidig)
Sent:	Monday, December 12, 1994 4:51 PM
To:	'paulp (Paul Poenisch)'
Cc:	'cadettes'; 'tbr (Tim B. Robinson)'; 'geert (Geert Rosseel)'; 'tom (Thomas Laidig)'
Subject:	active mask for well ties

I'd like to nail down a plan for what we're going to do with the existing 0.5 micron square well ties in euterpe. Since we're already supposed to have the baseplate finished, and any corrections we make will affect the baseplate layers, I think it's pretty urgent that we come to a conclusion quickly.

First let me summarize the background for those who haven't heard (and make sure I have it right).

The basic problem is that minimum-size features in the active mask print small, and don't reliably create openings in field oxide. The situation basically only arises with well ties. Currently, well ties (and collector connections) are drawn with a geometry on a single layer, collector-plug, which implies geometry on the active mask and on the collector plug implant mask. There are also some capacitors where we want the collector plug implant without any feature on the active
mask: this is drawn by adding geometry on the low-cap layer (which has no other use).

It is desirable to increase the drawn size of the active opening for a well tie without increasing the size of the collector implant. One reason is that this is a widely-diffusing implant and has large design rules. Another is that, even if drawn to meet design rules, this implant will diffuse outward enough to subtly alter the characteristics of pmos devices; drawing it minimum size minimizes this effect.

OK, so now we come to the question of what to do. It seems we have two, fairly independent, decisions to make:

    Keep the existing synthesis flow, and just draw additional geometry
    where we want the added active mask area -or- change the flow so the
    drawn collector plug simply defines the implant, and the active mask
    is explicitly drawn on another layer.

    Use Nactive for the (addtional or total) active geometry around well
    ties (and bipolar collectors) -or- define a new layer for this.

I suggest that we make the first decision in favor of explicitly drawing the active geometry on another layer. This simplifies the meaning of the drawn layers, and allows us to retire the low-cap layer entirely.
With little effort, we can automatically run over our entire design database to add the extra active geometry. Note that, whichever way we make this decision, we'll need to fix virtually all well ties manually.
I count 273 cells in proteus that contain collector-plug geometry, and most of these are well ties.

I suggest we make the second decision in favor of reusing the Nactive layer; I don't believe there is a need to define an additional layer for this. I think the only reason an additional layer might be desired is to simplify the identification of where N+ and P+ implants go. I think we already have enough stuff in the synthesis flow identifying areas close to collector-plug, that it would be simple to distinguish the implant treatment of the different Nactive areas.

Comments?

--
     ooooO   Ooooo
    (_)   (_)
     \(tau)/
     (_)   (_)

From: geert (Geert Rosseel)
Sent: Monday, December 12, 1994 5:36 PM
To: 'craig'; 'mouss'; 'tbr'
Subject: Re: CMOS euterpe

How about meeting on Tuesday 2:00 p.m. ?

       Geert

From: paulp (Paul Poenisch)

Sent: Monday, December 12, 1994 6:16 PM

To: 'Tom Laidig'

Cc: 'cadettes'; 'geert (Geert Rosseel)'; 'tbr (Tim B. Robinson)'; 'Paul Poenisch'

Subject: Re: active mask for well ties

> Tom Laidig writes:
>
> I'd like to nail down a plan for what we're going to do with the
> existing 0.5 micron square well ties in euterpe. Since we're already
> supposed to have the baseplate finished, and any corrections we make
> will affect the baseplate layers, I think it's pretty urgent that we
> come to a conclusion quickly.
>
> First let me summarize the background for those who haven't heard (and
> make sure I have it right).
>
> The basic problem is that minimum-size features in the active mask
> print small, and don't reliably create openings in field oxide. The
> situation basically only arises with well ties. Currently, well ties
> (and collector connections) are drawn with a geometry on a single
> layer, collector-plug, which implies geometry on the active mask and on
> the collector plug implant mask. There are also some capacitors where
> we want the collector plug implant without any feature on the active
> mask: this is drawn by adding geometry on the low-cap layer (which has
> no other use).

Actually I think that low-cap may be used but LVS (or is it NVL, I can never
remember which acranym we use here) to identify certain capacitors.
>
> It is desirable to increase the drawn size of the active opening for a
> well tie without increasing the size of the collector implant. One
> reason is that this is a widely-diffusing implant and has large design
> rules. Another is that, even if drawn to meet design rules, this
> implant will diffuse outward enough to subtly alter the characteristics
> of pmos devices; drawing it minimum size minimizes this effect.
>
> OK, so now we come to the question of what to do. It seems we have two,
> fairly independent, decisions to make:
>
>   Keep the existing synthesis flow, and just draw additional geometry
>   where we want the added active mask area -or- change the flow so the
>   drawn collector plug simply defines the implant, and the active mask
>   is explicitly drawn on another layer.
>
>   Use Nactive for the (addtional or total) active geometry around well
>   ties (and bipolar collectors) -or- define a new layer for this.
>
> I suggest that we make the first decision in favor of explicitly drawing
> the active geometry on another layer. This simplifies the meaning of
> the drawn layers, and allows us to retire the low-cap layer entirely.
> With little effort, we can automatically run over our entire design
> database to add the extra active geometry. Note that, whichever way we
> make this decision, we'll need to fix virtually all well ties manually.
> I count 273 cells in proteus that contain collector-plug geometry, and

> most of these are well ties.

I agree that this is probably easier than the other methods we've discussed
to date (modifying the flow to generate the extra active layer automatically
by several different methods). However getting rid of low-cap may cause
problems if it is used in LVS.
>
> I suggest we make the second decision in favor of reusing the Nactive
> layer; I don't believe there is a need to define an additional layer for
> this. I think the only reason an additional layer might be desired is
> to simplify the identification of where N+ and P+ implants go. I think
> we already have enough stuff in the synthesis flow identifying areas
> close to collector-plug, that it would be simple to distinguish the
> implant treatment of the different Nactive areas.

Using Nactive could lead to some fairly serious design rule problems, ie.
Nactive can not nomally be adjacent to Ppoly or Base poly (because of select
implant problems). Collector plugs are commonly placed adjacent to Ppoly and
Base poly, the problem is avoided by some fairly complex adjustments to the
P+ implant mask and by using the Emitter implant to dope the Collector plug
active layers. Using Nactive to expand the Collector plug active area would
require that the DRC program be able to distinguish Nactive used to expand
Collector plug from other Nactive areas which are not associated with Collector
plug. I suspect that this will be troublesome, therefore I think that a
separate layer should probably be used rather than Nactive.
>
> Comments?
>
> --
>   ooooO Ooooo
>   (_) (_)
>   \(tau)/
>   () ()
>

Paul.

From:	tbr
Sent:	Monday, December 12, 1994 10:39 PM
To:	'stick (Bruce Bateman)'
Cc:	'agc'; 'bpw'; 'geert'
Subject:	mnemo clock speed and sram write pulse
Follow Up Flag:	Follow up
Flag Status:	Red

Bruce Bateman wrote (on Mon Dec 12):

There seems to be some uncertainty about what the mnemo clock
rate will be - 1.297GHz (771ps tick) or 1.080GHz (926ps tick).
Please note that this impacts the control of the memory blocks
in terms of how many ticks wide the write pulse must be.

The original sim's were done with a 771ps tick and indicated
that a 3-tick write pulse (2.313ns) failed to write successfully
at 2.9v, 127C, and -3 sigma (i.e. - slow) distribution for
the N, P, and B hspice models. A 4-tick pulse (3.084ns) passed.

When the sim was changed to a 926ps tick, the 3-tick write pulse
(2.779ns) passed in all process/voltag/temp corners.

Thus, if we think there is a possibility that the interface to
the memory blocks will operate at the 1.297GHz (771ps tick) clock
rate, we need to design the logic to use a 4-tick write pulse to
insure that the memory array will work in all process corners.
Given the above data, a 3-tick pulse would be sufficient for
clock rates up to some point faster than 1.080GHz (926ps tick)
but slower than 1.297GHz (771ps tick). If necessary, the point
where the 3-tick pulse fails can be determined more accurately.

Unless it adds to overal latency, let's use a 4 tick pulse. That will
give us more flexibility. However, is the assumption of a 5 tick read
latency still good at 771? I would expect we end up running at 926
though, first because we are using the same cells as on euterpe and
it's not possible to make timing at 771 there. Second we will not be able
to run Mnemo faster than Euterpe.

Tim

I've been experimenting with inlining DES into several different drivers. One thing I
noticed is that it isn't moving all of the constant loads outside of the outer loop, which
is clearly preferable in these cases since it has enough free registers).

The top-level source is ~karzes/des/terp/ofb64_nd.c. Here's the inlined code for the
inner and outer loops. Notice the 5 constant loads at the bottom of the outer loop.
These loads should be performed outside of the outer loop.

```
.LLB1:
        eshufflei4mux   r6,r3,r24,8,1,2
        ecopyi          r3,0
        etranspose8mux  r7,r6,r38,r22
        ecopyi          r6,120
        etranspose8mux  r7,r7,r40,r20
        gshufflei       r10,r28,r7,128,16,4
        eselect8        r8,r7,r39

.LLB0.0:
                eshufflei4mux   r7,r8,r18,16,4,2
                l64l            r3,r2,r3
                etranspose8mux  r7,r7,r33,r16
                gcopyswapi      r34,r10,127,16
                exor            r13,r7,r3
                euwthi          r10,r13,6,24
                euwthi          r8,r13,6,6
                euwthi          r9,r13,6,12
                euwthi          r3,r13,6,18
                euwthi          r12,r13,6,36
                euwthi          r11,r13,6,30
                euwthi          r7,r13,6,0
                euwthi          r13,r13,6,42
                lu8             r15,r31,r10
                eaddi           r6,r6,-8
                lu8             r10,r29,r8
                lu8             r8,r30,r9
                lu8             r9,r32,r12
                lu8             r36,r30,r3
                exori           r3,r6,120
                lu8             r37,r32,r13
                lu8             r14,r29,r7
                gmdepi64        r36,r8,4,0
                lu8             r11,r31,r11
                gmdepi64        r10,r14,4,0
                gmdepi64        r10,r36,8,8
                gxor            r10,r10,r34
                gselect8        r8,r11,r10,r27
                bgez            r6,.LLB0.0

        gshufflei       r10,r11,r10,128,16,2
        l128li          r12,dp,.L15-_._ofb64_nd
        eshli           r8,r26,3
        l64li           r9,dp,.L16-_._ofb64_nd
        eshufflei4mux   r3,r10,r12,64,1,8
        l128li          r6,dp,.L17-_._ofb64_nd
        eaddi           r26,r26,1
        etranspose8mux  r3,r3,r9,r6
        l64li           r9,dp,.L18-_._ofb64_nd
        l128li          r6,dp,.L19-_._ofb64_nd
```

```
etranspose8mux  r3,r3,r9,r6
s64l            r3,r4,r8
bl              r26,r5,.LLB1
```

From: chip (Buffalo Chip)
Sent: Tuesday, December 13, 1994 4:01 AM
To: 'geert'
Subject: pager log message

```
page from chip to geert:
Release euterpe/verilog/bsrc/rgxmit BOM 18.0 initiated by mws completed @ Tue Dec 13
01:59:47 PST 1994 with exit status 0.. chip
```

From:	chip (Buffalo Chip)
Sent:	Tuesday, December 13, 1994 4:16 AM
To:	'geert'
Subject:	pager log message

page from chip to geert:
Release euterpe/verilog/bsrc/rg BOM 91.0 initiated by mws completed @ Tue Dec 13 02:15:17
PST 1994 with exit status 1.. chip

From: woody (Jay Tomlinson)
Sent: Tuesday, December 13, 1994 10:27 AM
To: 'tbr'
Cc: 'woody'
Subject: pandora boards

Tim,

boards for Pandora are:

main board that will contain:
    1 euterpe
    4 mnemo daughter boards
    ??1 pci daughter board
    assoc connectors

mnemo (daughter) board that will contain:
    1 mnemonsyne
    ram
    assoc. connectors

pci (daughter??) board that will contain:
    1 mnemonsyne
    assoc connectors for connecting to PCI bus.

calliope board that will contain:
    1 calliope
    assoc connectors

The output from euterpe/verilog/bsrc/cdio/.checkoutrc is 160k, so it is not included in
this mail message. Instead, check the file

/n/tmp/chiplog/geert.godzilla.12834.euterpe-verilog-bsrc-cdio

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

From:	Buffalo Chip [chip@rhea]
Sent:	Tuesday, December 13, 1994 11:13 AM
To:	'geert@rhea'
Subject:	pager log message

```
page from chip to geert:
Release euterpe/verilog/bsrc/cdio BOM 37.0 initiated by geert completed @ Tue Dec 13
09:12:13 PST 1994 with exit status 0.. chip
```

From:	Buffalo Chip [chip@godzilla]
Sent:	Tuesday, December 13, 1994 11:38 AM
To:	'geert@godzilla'
Subject:	output of euterpe/verilog/bsrc/ctiod/.checkoutrc

The output from euterpe/verilog/bsrc/ctiod/.checkoutrc is 152k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.godzilla.15314.euterpe-verilog-bsrc-ctiod

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

From:	chip (Buffalo Chip)
Sent:	Tuesday, December 13, 1994 1:37 PM
To:	'geert'
Subject:	output of euterpe/verilog/bsrc/ctioi/.checkoutrc

The output from euterpe/verilog/bsrc/ctioi/.checkoutrc is 160k, so it is not included in
this mail message. Instead, check the file

/n/tmp/chiplog/geert.gamorra.13759.euterpe-verilog-bsrc-ctioi

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

The output from euterpe/verilog/bsrc/hz/.checkoutrc is 136k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.godzilla.20647.euterpe-verilog-bsrc-hz

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

From:	Buffalo Chip [chip@rhea]
Sent:	Tuesday, December 13, 1994 4:19 PM
To:	'geert@rhea'
Subject:	pager log message

```
page from chip to geert:
Release euterpe/verilog/bsrc/lt BOM 73.0 initiated by geert completed @ Tue Dec 13
14:17:50 PST 1994 with exit status 0.. chip
```

From: Loretta Guarino [guarino@MicroUnity.com]

Sent: Tuesday, December 13, 1994 5:39 PM

To: 'sysadmin@MicroUnity.com'; 'lisar@MicroUnity.com'

Subject: who's responsible for man page installation?

Forwarded message:
```
> From gnats@rhea Mon Dec 12 16:00:05 1994
> Date: Mon, 12 Dec 1994 16:00:02 -0800
> Message-Id: <199412130000.QAA01932@rhea.microunity.com>
> From: brianl@MicroUnity.com (Brian Lee)
> Reply-To: brianl@MicroUnity.com (Brian Lee)
> To: vandyke@rhea
> Cc: lisa@rhea
> Subject: othertools/1803: frame man page not world readable
> In-Reply-To: Your message of Mon, 12 Dec 1994 15:51:32 -0800
>     <199412122351.PAA11426@ghidra.microunity.com>
>
>
> >Number:       1803
> >Category:     othertools
> >Synopsis:     frame man page not world readable
> >Confidential: yes
> >Severity:     non-critical
> >Priority:     low
> >Responsible:  vandyke (Don Van Dyke)
> >State:        open
> >Class:        support
> >Submitter-Id: MUSE
> >Arrival-Date: Mon Dec 12 16:00:01 1994
> >Originator:   Brian Lee
> >Organization:
> MicroUnity Systems Engineering, Inc.
> >Release:      unknown-1.0
> >Environment:
> System: SunOS ghidra 4.1.3 16 sun4m
> Architecture: sun4
>
> >Description:
> >How-To-Repeat:
> brianl@ghidra 411% man frame
> /usr/local/man/mann/frame.n: Permission denied
> brianl@ghidra 412% dv
> 0     ~/chip/euterpe/doc
> 1     ~/chip/euterpe/verilog/bsrc/sr
> brianl@ghidra 413% ll /usr/local/man/mann/frame.n
>   10 -r--r----- 1 root        9247 Oct 28 14:42 /usr/local/man/mann/frame.n
>
> >Fix:
> >Audit-Trail:
> >Unformatted:
>
>
>
```

------- End of Forwarded Message

From: ken (Ken Hsieh)

Sent: Tuesday, December 13, 1994 5:58 PM

To: 'guarino@MicroUnity.com'

Cc: 'lisa'; 'sysadm'; 'lisar'

Subject: Re: who's responsible for man page installation?

Fixed.

Ken

```
> From guarino@thessalus.microunity.com Tue Dec 13 15:39:01 1994
> To: sysadmin@thessalus.microunity.com, lisar@thessalus.microunity.com
> Subject: who's responsible for man page installation?
> Date: Tue, 13 Dec 94 15:38:53 -0800
> From: Loretta Guarino <guarino@thessalus.microunity.com>
> Content-Length: 1432
>
>
> Forwarded message:
> > From gnats@rhea Mon Dec 12 16:00:05 1994
> > Date: Mon, 12 Dec 1994 16:00:02 -0800
> > Message-Id: <199412130000.QAA01932@rhea.microunity.com>
> > From: brianl@MicroUnity.com (Brian Lee)
> > Reply-To: brianl@MicroUnity.com (Brian Lee)
> > To: vandyke@rhea
> > Cc: lisa@rhea
> > Subject: othertools/1803: frame man page not world readable
> > In-Reply-To: Your message of Mon, 12 Dec 1994 15:51:32 -0800
> >      <199412122351.PAA11426@ghidra.microunity.com>
> >
> >
> > >Number:       1803
> > >Category:     othertools
> > >Synopsis:     frame man page not world readable
> > >Confidential: yes
> > >Severity:     non-critical
> > >Priority:     low
> > >Responsible:  vandyke (Don Van Dyke)
> > >State:        open
> > >Class:        support
> > >Submitter-Id:  MUSE
> > >Arrival-Date:  Mon Dec 12 16:00:01 1994
> > >Originator:    Brian Lee
> > >Organization:
> > MicroUnity Systems Engineering, Inc.
> > >Release:       unknown-1.0
> > >Environment:
> > System: SunOS ghidra 4.1.3 16 sun4m
> > Architecture: sun4
> >
> > >Description:
> > >How-To-Repeat:
> > brianl@ghidra 411% man frame
> > /usr/local/man/mann/frame.n: Permission denied
```

```
> > brianl@ghidra 412% dv
> > 0    ~/chip/euterpe/doc
> > 1    ~/chip/euterpe/verilog/bsrc/sr
> > brianl@ghidra 413% ll /usr/local/man/mann/frame.n
> >   10 -r--r----- 1 root      9247 Oct 28 14:42 /usr/local/man/mann/frame.n
> >
> > >Fix:
> > >Audit-Trail:
> > >Unformatted:
> >
> >
> >
>
>
> ------- End of Forwarded Message
>
>
```

What's the current status of iobytem? The most recent build of the proteus snapshot has failed in the ged2verilog conversion of iobytem:

MicroUnity Spice Interface Version 1.93 No Copyright (C) 1990 Valid Logic Systems, Inc.

```
Processing Scald directories                              (00:00:00.78)
Calling ValidCompiler ...
Reading logical database                                  (00:00:26.22)
```

Verilog option is ON.
        Collapsing Interface vectors into busses

```
Reading /n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/iockdrvm.v
for IOCKDRVM
Reading /n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/iocdr2pm.v
for IOCDR2PM
ERROR! Verilog ckfq_alph pin in IOCDR2PM.V has no corresponding GED pin.
ERROR! Verilog ckfq_blph pin in IOCDR2PM.V has no corresponding GED pin.
Reading /n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/iocvrm.v
for IOCVRM
Reading /n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/nullbody.v
for IOCSSEL
Reading /n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/iovrrswm.v
for IOVRRSWM
Reading /n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/ioplatm.v
for IOPLATM
Reading /n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/ioskewbuf.v
for IOSKEWBUF
Reading
/n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/iomux8cdh10s.v for IOMUX8CDH10S
Reading /n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/nullbody.v
for IOBELLYBUTT
Reading
/n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/iocsbuffer.v for IOCSBUFFER Reading
/n/auspex/s23/euterpe-proteus-cp/proteus/verilog/dclib/ioploutm.v
for IOPLOUTM
```

Number of ERRORS found: 2

Tim

B. P. Wong wrote (on Tue Dec 13):

> Unless it adds to overal latency, let's use a 4 tick pulse. That will
> give us more flexibility. However, is the assumption of a 5 tick read
> latency still good at 771? I would expect we end up running at 926
> though, first because we are using the same cells as on euterpe and
> it's not possible to make timing at 771 there. Second we will not be able
> to run Mnemo faster than Euterpe.
>
> Tim
>
The read access time will work in 5 ticks, however, we would like to
have at least 1 tick address setup to WE and 1 tick address hold after
WE for recovery. If we are going to 4 ticks WE then we should plan for
6 ticks cycle.

Don't confuse reads with writes! The writes always happen immediately after a read and to
the same address, so there is no problem with address setup time. The cycle time for
writes is actually limited by the length of the write packets which take 14 clocks, so we
are unlikely to be limited by the cycle time in that case.

Tim

From:	tbr
Sent:	Tuesday, December 13, 1994 10:03 PM
To:	'woody (Jay Tomlinson)'
Cc:	'woody'
Subject:	pandora boards
Follow Up Flag:	Follow up
Flag Status:	Red

Jay Tomlinson wrote (on Tue Dec 13):

Tim,

boards for Pandora are:

main board that will contain:
    1 euterpe
    4 mnemo daughter boards
    ??1 pci daughter board
    assoc connectors

Actually it's looking like we need more modularity.
It is attractive to figure a way to put the euterpe on a
module too. We need a little more time now David is on board to
sketch out a plan. There are some hard thermal problems to solve.

mnemo (daughter) board that will contain:
    1 mnemonsyne
    ram
    assoc. connectors

Will also need buffers for 3-5V conversion.

pci (daughter??) board that will contain:
    1 mnemonsyne
    assoc connectors for connecting to PCI bus.

Not clear if this can be a module yet.

calliope board that will contain:
    1 calliope
    assoc connectors

Plus a comparable bag of analog as on Hestia. There is a way to go to
get this defined!

Tim

From: woody (Jay Tomlinson)

Sent: Tuesday, December 13, 1994 10:18 PM

To: 'tbr (Tim B. Robinson)'

Subject: pandora boards

Tim B. Robinson wrote (on Tue Dec 13):

Jay Tomlinson wrote (on Tue Dec 13):

Tim,

boards for Pandora are:

main board that will contain:
    1 euterpe
    4 mnemo daughter boards
    ??1 pci daughter board
    assoc connectors

Actually it's looking like we need more modularity.
It is attractive to figure a way to put the euterpe on a
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sketch out a plan. There are some hard thermal problems to solve.

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    1 mnemonsyne
    ram
    assoc. connectors

Will also need buffers for 3-5V conversion.

pci (daughter??) board that will contain:
    1 mnemonsyne
    assoc connectors for connecting to PCI bus.

Not clear if this can be a module yet.

calliope board that will contain:
    1 calliope
    assoc connectors

Plus a comparable bag of analog as on Hestia. There is a way to go to
get this defined!

Tim

Last week you wanted me to put together a netlist. I think it was for mnemo
board. Do you still want that, or should I forget it for now?
Jay

From: tbr

Sent: Tuesday, December 13, 1994 11:12 PM

To: 'wayne (Wayne Freitas)'

Cc: 'albers'; 'pmayer'; 'philip'; 'hestia'

Subject: Mainboard status

Follow Up Flag: Follow up

Flag Status: Red

Wayne Freitas wrote (on Tue Dec 13):

> Tim, can you provide me some information to what happened to Main Board,
> and how long its going to take before the gerbers go out. Also are we going to
> spend the time to correct the problem in the VCO section?

The main problem was inadequate clearances in the inner layers caused
by two things. First, we misinterpreted hadco's requirement of 22
mils clearance over the drill size as 22 mils overal. This gave us 5
mils less clearence than they were comfortable with. Second, for some
reason, PCAD drew the clearances as hexagons (irregular ones at that),
such that the 22 mils was across the diagonal. Across the flats we
lost a few more mils. DRC had not picked this up. The design
guidelines document has been amended to correct this.

At first Hadco thought it could be fixed by a reduction in drill size
to 8 mils and a change to the etch profile. However, they
subsequently backed off that. We thought we could fix it by massaging
the ASCII files but dan had trouble getting good results (Gerber's
looked OK, but pcad thought the resulting database was corrupt). We
had no option but to open the data base and fix it properly. However,
we are restricting the changes to the inner layer clearances in view
of the fact that PCAD is so fragile. Now, this introduces a new
problem. Putting in the clearances cuts slots in the ground plane to
the right of euterpe, (and to a lesser extent in other places). Since
we expect the main value of this first batch of boards to be for the
manufacturing and analog issues we decided to accept this even though
it may compromise signal quality on the SDRAM interface. In the
Allegro version we will have to re-rout all the traces in that area in
order to spread the vias apart, and we expect to have boards from
the Allegro version in time for Euterpe.

Estimated hit for all this was 2 days (we are trying to minimise work
as it's delaying the Allegro conversion), but I have not had a chance
today to check the progress. I had also overlooked the VCO issue, and
if the changes have not been completed we should consider adding the
missing vias if pattie thinks that will not compromise the database.
We will of course have to re-run DRC as part of this.

Tim

From: tbr (Tim B. Robinson)
Sent: Tuesday, December 13, 1994 11:12 PM
To: 'wayne (Wayne Freitas)'
Cc: 'albers'; 'pmayer'; 'philip'; 'hestia'
Subject: Mainboard status

Wayne Freitas wrote (on Tue Dec 13):

>   Tim, can you provide me some information to what happened to Main Board,
>   and how long its going to take before the gerbers go out. Also are we going to
>   spend the time to correct the problem in the VCO section?

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First, we misinterpreted hadco's requirement of 22 mils clearance over the drill size as
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Second, for some reason, PCAD drew the clearances as hexagons (irregular ones at that),
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DRC had not picked this up.   The design guidelines document has been amended to correct
this.

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(Gerber's looked OK, but pcad thought the resulting database was corrupt). We had no
option but to open the data base and fix it properly. However, we are restricting the
changes to the inner layer clearances in view of the fact that PCAD is so fragile. Now,
this introduces a new problem. Putting in the clearances cuts slots in the ground plane
to the right of euterpe, (and to a lesser extent in other places). Since we expect the
main value of this first batch of boards to be for the manufacturing and analog issues we
decided to accept this even though it may compromise signal quality on the SDRAM
interface.   In the Allegro version we will have to re-rout all the traces in that area in
order to spread the vias apart, and we expect to have boards from the Allegro version in
time for Euterpe.

Estimated hit for all this was 2 days (we are trying to minimise work as it's delaying the
Allegro conversion), but I have not had a chance today to check the progress. I had also
overlooked the VCO issue, and if the changes have not been completed we should consider
adding the missing vias if pattie thinks that will not compromise the database.
We will of course have to re-run DRC as part of this.

Tim

From: tbr

Sent: Tuesday, December 13, 1994 11:15 PM

To: 'ken (Ken Hsieh)'

Cc: 'sysadm'

Subject: Re: who's responsible for man page installation?

Follow Up Flag: Follow up

Flag Status: Red

Was this wrong on all the sparc 10's or just ghidra?

Ken Hsieh wrote (on Tue Dec 13):

Fixed.

Ken

> From guarino@thessalus.microunity.com Tue Dec 13 15:39:01 1994
> To: sysadmin@thessalus.microunity.com, lisar@thessalus.microunity.com
> Subject: who's responsible for man page installation?
> Date: Tue, 13 Dec 94 15:38:53 -0800
> From: Loretta Guarino <guarino@thessalus.microunity.com>
> Content-Length: 1432
>
>
> Forwarded message:
> > From gnats@rhea Mon Dec 12 16:00:05 1994
> > Date: Mon, 12 Dec 1994 16:00:02 -0800
> > Message-Id: <199412130000.QAA01932@rhea.microunity.com>
> > From: brianl@MicroUnity.com (Brian Lee)
> > Reply-To: brianl@MicroUnity.com (Brian Lee)
> > To: vandyke@rhea
> > Cc: lisa@rhea
> > Subject: othertools/1803: frame man page not world readable
> > In-Reply-To: Your message of Mon, 12 Dec 1994 15:51:32 -0800
> >   <199412122351.PAA11426@ghidra.microunity.com>
> >
> >
> > >Number: 1803
> > >Category: othertools
> > >Synopsis: frame man page not world readable
> > >Confidential: yes
> > >Severity: non-critical
> > >Priority: low
> > >Responsible: vandyke (Don Van Dyke)
> > >State: open
> > >Class: support
> > >Submitter-Id: MUSE
> > >Arrival-Date: Mon Dec 12 16:00:01 1994
> > >Originator: Brian Lee
> > >Organization:
> > MicroUnity Systems Engineering, Inc.
> > >Release: unknown-1.0
> > >Environment:

```
> > System: SunOS ghidra 4.1.3 16 sun4m
> > Architecture: sun4
> >
> > >Description:
> > >How-To-Repeat:
> > brianl@ghidra 411% man frame
> > /usr/local/man/mann/frame.n: Permission denied
> > brianl@ghidra 412% dv
> > 0     ~/chip/euterpe/doc
> > 1     ~/chip/euterpe/verilog/bsrc/sr
> > brianl@ghidra 413% ll /usr/local/man/mann/frame.n
> >  10 -r--r----- 1 root     9247 Oct 28 14:42 /usr/local/man/mann/frame.n
> >
> > >Fix:
> > >Audit-Trail:
> > >Unformatted:
> >
> >
> >
> 
> 
> ------- End of Forwarded Message
> 
> 
```

From:	chip (Buffalo Chip)
Sent:	Wednesday, December 14, 1994 12:14 AM
To:	'geert'
Subject:	output of euterpe/verilog/bsrc/cc/.checkoutrc

The output from euterpe/verilog/bsrc/cc/.checkoutrc is 160k, so it is not included in this mail message. Instead, check the file

/n/tmp/chiplog/geert.tomato.15765.euterpe-verilog-bsrc-cc

(which is accessible from all machines). This file will disappear in about 5 days.

By the way, the exit status returned by .checkoutrc was 0.

From:	Buffalo Chip [chip@rhea]
Sent:	Wednesday, December 14, 1994 1:52 AM
To:	'geert@rhea'
Subject:	pager log message

page from chip to geert:
Release euterpe/verilog/bsrc/at BOM 30.0 initiated by woody completed @ Tue Dec 13
23:50:24 PST 1994 with exit status 0.. chip

From:	Buffalo Chip [chip@rhea]
Sent:	Wednesday, December 14, 1994 2:03 AM
To:	'geert@rhea'
Subject:	pager log message

```
page from chip to geert:
Release euterpe/verilog/bsrc/sr BOM 44.0 initiated by brianl completed @ Wed Dec 14
00:01:56 PST 1994 with exit status 0... chip

all ports busy
```

From: Buffalo Chip [chip@rhea]
Sent: Wednesday, December 14, 1994 8:31 AM
To: 'geert@rhea'
Subject: pager log message

```
page from chip to geert:
Release euterpe/verilog/bsrc/nb BOM 89.0 initiated by hopper completed @ Wed Dec 14
06:29:23 PST 1994 with exit status 1.. chip
```

From: billz (Bill Zuravleff)
Sent: Wednesday, December 14, 1994 9:50 AM
To: 'geert'
Subject: Re: cc failed in /u/chip

Failure? I see this in
/u/chip/euterpe/verilog/bsrc/cc/gards/cc-final.topt.log:

```
Atoms:              count   atom    bjt isrc   pld clock
      BJT Totals:  746 8426      14621   10194    14508    7049


   Congratulations!  No timing or DC Load violations!
```

It completed after your message was sent. So maybe check again (?).
billz

From: ken (Ken Hsieh)

Sent: Wednesday, December 14, 1994 10:46 AM

To: 'tbr'

Cc: 'sysadm'

Subject: Re: who's responsible for man page installation?

Tim,

I was wrong on all sparc 10's.

Ken

> From tbr Tue Dec 13 21:15:28 1994
> Date: Tue, 13 Dec 1994 21:15:26 -0800
> From: tbr (Tim B. Robinson)
> To: ken (Ken Hsieh)
> Cc: sysadm
> Subject: Re: who's responsible for man page installation?
> Content-Length: 2151
>
>
> Was this wrong on all the sparc 10's or just ghidra?
>
> Ken Hsieh wrote (on Tue Dec 13):
>
>   Fixed.
>
>   Ken
>
>   > From guarino@thessalus.microunity.com Tue Dec 13 15:39:01 1994
>   > To: sysadmin@thessalus.microunity.com, lisar@thessalus.microunity.com
>   > Subject: who's responsible for man page installation?
>   > Date: Tue, 13 Dec 94 15:38:53 -0800
>   > From: Loretta Guarino <guarino@thessalus.microunity.com>
>   > Content-Length: 1432
>   >
>   >
>   > Forwarded message:
>   > > From gnats@rhea Mon Dec 12 16:00:05 1994
>   > > Date: Mon, 12 Dec 1994 16:00:02 -0800
>   > > Message-Id: <199412130000.QAA01932@rhea.microunity.com>
>   > > From: brianl@MicroUnity.com (Brian Lee)
>   > > Reply-To: brianl@MicroUnity.com (Brian Lee)
>   > > To: vandyke@rhea
>   > > Cc: lisa@rhea
>   > > Subject: othertools/1803: frame man page not world readable
>   > > In-Reply-To: Your message of Mon, 12 Dec 1994 15:51:32 -0800
>   > >   <199412122351.PAA11426@ghidra.microunity.com>
>   > >
>   > >
>   > > >Number: 1803
>   > > >Category: othertools
>   > > >Synopsis: frame man page not world readable
>   > > >Confidential: yes

```
>    > > >Severity:     non-critical
>    > > >Priority:     low
>    > > >Responsible:   vandyke (Don Van Dyke)
>    > > >State:        open
>    > > >Class:        support
>    > > >Submitter-Id:  MUSE
>    > > >Arrival-Date:  Mon Dec 12 16:00:01 1994
>    > > >Originator:   Brian Lee
>    > > >Organization:
>    > > MicroUnity Systems Engineering, Inc.
>    > > >Release:      unknown-1.0
>    > > >Environment:
>    > > System: SunOS ghidra 4.1.3 16 sun4m
>    > > Architecture: sun4
>    > >
>    > > >Description:
>    > > >How-To-Repeat:
>    > > brianl@ghidra 411% man frame
>    > > /usr/local/man/mann/frame.n: Permission denied
>    > > brianl@ghidra 412% dv
>    > > 0     ~/chip/euterpe/doc
>    > > 1     ~/chip/euterpe/verilog/bsrc/sr
>    > > brianl@ghidra 413% ll /usr/local/man/mann/frame.n
>    > >  10 -r--r----- 1 root      9247 Oct 28 14:42 /usr/local/man/mann/frame.n
>    > >
>    > > >Fix:
>    > > >Audit-Trail:
>    > > >Unformatted:
>    > >
>    > >
>    > >
>    >
>    >
>    > ------- End of Forwarded Message
>    >
>    >
>
```

```
              Software Bringup Meeting
              ------------------------
                  December 14, 1994

Next Meeting:      December 21 at 10:00 am.

Attendees:  jeffm, guarino, gmo, doi, sandeep, wayne


New Action Items
---------------------------------------------------------------------
-

Item: Implement parallel port device driver for Lynix on PC.
Who:  jerry, doi
Status:     [12/14] New.

Item: Get cycle counts/differences for the oc-mem tests that lisar ran.
Who:  doi
Status:     [12/14] New.

Item: Get cycle counts of kernel tests to jeffm
Who:  guarino
Status:     [12/14] New.


Review of Action Items
---------------------------------------------------------------------
---

Item: SW simulator has to be updated to reflect the new event daemon
      space.
Who:  gmo
Status:     [12/07] Done.

Item: Once the SW simulator has been updated to reflect the new event
      daemon space, some software will have to be changed too.
Who:  jeffm, guarino, sandeep
Status:     [12/07] Done.

Item: Define and implement a snapshot environment for the HW and SW
      simulators.
Who:  jeffm, gmo
Status:     [11/30] In progress

      Jeff is going to start the process off with an e-mail message
      summarizing the current thoughts on the subject.

Item: Continue trying to find either source code for parallel drivers
      or descriptions of hardware so we can write out own.
Who:  gmo   sgi machines
Who:  doi   sun machines
Status:     [11/23] progress continues.

      Expect info about Sun drivers from Acclaim (still).
      Expect info about SGI drivers from another vendor (still).
      Wayne says that National does not provice source for Suns but
```

does for PCs and Macs.

Item: Implement parallel port device drivers for sun and sgi.
Who: sandeep, doi
Status: Dropped.

       Wait until we find the results of the `quest for Sun/Sgi source'
       and the results of the device driver on the PC running Lynix.

Item: Build scripting/UI capabilities above gdb for regression tests.
Who: doi
Status: on hold until the the boot, gdb boot stub, and virtual devices
       are complete. (estimated start date of 12/23)

Item: Create performance test plan
Who: jeffm, guarino
Status: [11/30] no progress

Item: Add Unix-like tests to software acceptance tests.
Who: iimura
Status: [11/30] In progress.

       Wally has been spending time looking at why the kernel
       does not run with terp with cycle counting enabled.

Item: Simulator needs to understand `reset'
Who: gmo
Status: [11/30] In progress.

Item: Implement and bring-up boot, gdb boot stub, and virtual device
       support on the software simulator.
Who: sandeep/gmo
Status: in progress (delayed until 1/10 from original target of 12/23)

       Changing the packet protocol to handle octlets instead
       of just bytes. This will introduce a week delay but the
       holidays will introduce about another week.

Test Status

-

Jeffm is looking at the failures reported with BOM 187.0-R1 (load/use fix) but his first
runs in his own environement have worked? Investigation continues.

Some initial tests running on the IKOS.

Jeffm has the sdram behavioral working with the IKOS.

From: ras (Bob Sutherland)

Sent: Wednesday, December 14, 1994 5:02 PM

To: 'ptolemy'

Subject: Minutes 12/14/94

Minutes ..

-Re-evaluated path from concept to ptolemy. It appears that
we can use a CAEViews translator to convert a concept database
to ptcl, thence to ptolemy. brianl did get a (semi-)
successful path through edif, but vanthof thinks the CAEViews
path should be relatively easy to construct. The advantages
are that the octtool database is circumvented and that this
paradigm fits in better with our existing concept methodology.
Dave has volunteered to write the translator.

-brian hasn't had much time to work with his socket interface,
but has passed the prototype effort off to brianl to try and
fix some dynamic link related bugs. When time is available,
he will continue with the PLL simulation example.

-It appears that we can accelerate in a distributed
environment by plugging DSP boards into the S-bus slots in the
sparcs. Unfortunately, the only card identified so far is
based on the AT&T DSP32C, and is not directly supported by the
Ptolemy group. The only floating point chip we know they
support is the Motorola DSP96002, which I can find only in
ISA (PC). The HP9000/730 (adder) supports an E(ISA)
expansion slot, but then it wouldn't be distributed. I'm
still collecting data.

There weren't many people at the meeting, but that's ok as there
wasn't alot of progress due to other time committments. We did,
however, discuss the overall simulation environment and have decided
that lisar and tbr's concept of a distributed network of independent
simulations of functional blocks, with sockets running to a hub
controller is entirely possible. We may even be able to do some
simulation of the communication protocols (under the CP domain) if we
stay within the Sun environment.

--
"No!No!.. Don't pull on that.. you never know what it's attached to."

RAS

From: geert (Geert Rosseel)

Sent: Wednesday, December 14, 1994 10:41 PM

To: 'billz'; 'dickson'; 'mws'; 'tbr'; 'woody'

Subject: Euterpe top-level

Hi,

I rebuild the toplevel and :

* at has a lot of xbhrdh24s and therefore is quite big. Can someone
  check the paths on these cells ?

* there seems to be a butterfly between sr and at . I don't know
  which one is inverted.

Toplevel is in /n/ghidra/s3/geert/euterpe/verilog/bsrc/gards/geert_euterpe-iter

                    Geert

From:	woody (Jay Tomlinson)
Sent:	Wednesday, December 14, 1994 11:45 PM
To:	'geert (Geert Rosseel)'
Cc:	'billz'; 'dickson'; 'mws'; 'tbr'
Subject:	Euterpe top-level

Geert Rosseel wrote (on Wed Dec 14):

    Hi,

    I rebuild the toplevel and :

       * at has a lot of xbhrdh24s and therefore is quite big. Can someone
         check the paths on these cells ?

/u/chip.../at/gards/at-iter.strength lists:
  fva (UxcLvaR13R14H:L/u31:u0) as 24s. This is a power.tab.local/top problem since this is
an hr->muxen->muxen-hr path to sr. In fact (somebody correct me if I am wrong) I think
these could be 2s since the data is loaded into the hr and re-circulates (mux-hr) for a
lot of cycles before it is actually used by sr.

  dtag (UctPaR12/u47:0) as 24s. This is currently a ff->muxff to cc, it could be an hr->
mux->hr path.

 phys address (Upa4700R12/u47:0) as 24s. This is currently a ff->muxff path to cc, it
could be an hr->mux->hr path if cc is allowed to use the 1st-cycle of the two. AT can't
back it up a cycle because this would increase loading on an already sensitive path from
the gtlb.

The above covers the bulk of the 24s cells in at. There are some scalar interfaces to UU
to report exceptions and some others to CC which are the control for above.

       * there seems to be a butterfly between sr and at . I don't know
         which one is inverted.

If this is a large butterfly (64 bits) then it is probably the fva mentioned above. at
places bit0 at the bottom and bit 63 at the top to reduce routing from gtlb to at/phys
address. I would expect sr to have the bits placed in the same order as the dickson's
datapath.

Jay

    Toplevel is in
/n/ghidra/s3/geert/euterpe/verilog/bsrc/gards/geert_euterpe-iter

                     Geert

From:	tbr
Sent:	Thursday, December 15, 1994 11:28 AM
To:	'fwo (Fred Obermeier)'
Cc:	'fwo'
Subject:	euterpe/verilog/bsrc/gards/tbr* files
Follow Up Flag:	Follow up
Flag Status:	Red

Fred Obermeier wrote (on Thu Dec 15):

Tim,

How does one generate euterpe/verilog/bsrc/gards/*euterpe* files?
The bsrc/Makefile doesn't know how to build this and neither do I.

I think you are probably hitting the problem with the
GARDS_SUBDIRS_1/2 settings.

Tim

From: woody (Jay Tomlinson)
Sent: Thursday, December 15, 1994 11:31 AM
To: 'tbr (Tim B. Robinson)'
Cc: 'billz (Bill Zuravleff)'; 'dickson (Richard Dickson)'; 'geeert'; 'Mark Semmelmeyer'
Subject: Re: Euterpe top-level

It turns out that the problems that geert mentioned are due to the fact that at
the toplevel topt is not allowed to power cells down (trying to avoid
thrashing). geert is rerunning at with topt set to power primary outputs to 4s
(or something small). Then when iterating at toplevel, the cells will power up
as needed.
Jay

Tim B. Robinson wrote (on Thu Dec 15):

  Mark Semmelmeyer wrote (on Wed Dec 14):

    woody wrote:

    > ... this is an hr->muxen->muxen-hr path to sr. In fact
    > (somebody correct me if I am wrong) I think these
    > could be 2s since the data is loaded into the hr and
    > re-circulates (mux-hr) for a lot of cycles before it is actually used by sr.

    I think we should be very sure we want to violate timing on logic paths.
    Normal usage would allow lots of cycles for the data to transmit,
    but software is still free to read the fva at any time. To keep
    such reads on architecturally visible paths deterministic, we would
    have to limit the paths to two ticks.

  I agree. It's already scary that we have multicycle paths in the
  arrays and we are building special models to detect algorithmic
  violations there. Let's not create more except in absolute desperation!

    > phys address (Upa4700R12/u47:0) as 24s. This is currently a ff->muxff path to
    > cc, it could be an hr->mux->hr path if cc is allowed to use the 1st-cycle of
    > the two.

    If cc is allowed to use the 1st cycle, then it is a one tick path
    and hr --> whatever --> hr does not help (in fact I believe gloss
    will flag it as a phase error).

  There was a case I think where addition of buffers allowed one path to
  be single cycle and another double cycle with a net saving because the
  double path was really easy (buffer goes in that path of course). Is
  this one amneable to similar treatment?

  Tim

From:	wingard (Drew Wingard)
Sent:	Thursday, December 15, 1994 12:48 PM
To:	'bill'; 'bpw'; 'geert'; 'stick'; 'vo'
Subject:	Simulation conditions

Geert and I were thinking that if we're going to head off to do a bunch of simulations, we ought to make sure we can compare results easily.

We therefore propose a 'standard' operating condition for simulation, namely stick and bpw's: 4.4V nominal CSM at 127C, i.e.

```
* Operating Conditions for Foundry Euterpe .lib
'/u/chip/proteus/technology/csm/hspice/models.lib' csm_60 .param op_temp=127 .param
op_vdd=4.4

.temp 'op_temp'
vdd    vdd    vss    dc    'op_vdd'
```

Happy Hacking,
Drew

From: Loretta Guarino [guarino@MicroUnity.com]

Sent: Thursday, December 15, 1994 12:59 PM

To: 'sysadmin@MicroUnity.com'

Cc: 'tbe@MicroUnity.com'; 'tbr@MicroUnity.com'; 'lisar@MicroUnity.com'; 'guarino@MicroUnity.com'

Subject: gnats problems

The entry for gnats-dist in /usr/lib/aliases has changed,
which is causing this failure. Instead of

"|/usr/local/lib/gnats/queue-pr-q > /dev/null 2>&1"

it should contain

"|/usr/local/lib/gnats/queue-pr -q > /dev/null 2>&1"

The -q is a switch, not part of the path name. Could you
please fix this?

I'll check to ensure that /usr/local/lib/gnats/queue-pr
exists on all the systems. At the moment, it appears to be
on the suns but not on the sgis.

Also, could someone please advise me how to get the new man
pages into the right location so that info will find them?
Info is still showing me the man pages for the old version
of gnats, and I'm sure this is an installation problem on my
part.

Thanks, Loretta

------- Forwarded Message

Return-Path: <tbr>
Received: from aphrodite.microunity.com by gaea.microunity.com (4.1/muse1.3)
        id AA16178; Wed, 14 Dec 94 19:18:45 PST
Received: from localhost by aphrodite.microunity.com (8.6.4/muse-sw.3)
        id TAA29566; Wed, 14 Dec 1994 19:25:54 -0800
Date: Wed, 14 Dec 1994 19:25:54 -0800
From: tbr (Tim B. Robinson)
Message-Id: <199412150325.TAA29566@aphrodite.microunity.com>
To: guarino
Subject: forwarded message from Tom Eich

- ------- Start of forwarded message -------
Status: RO
X-VM-v5-Data: ([nil nil t nil nil nil nil nil nil]
        ["2194" "Wed" "14" "December" "94" "17:35:21" "PST" "Tom Eich" "tbe@MicroUnity.com " nil "69" "Returned mail:
unknown mailer error 1" "^From:" nil nil "12"])
Return-Path: <tbe@MicroUnity.com>
Received: from [192.216.192.231] (randmac2.microunity.com) by gaea.microunity.com (4.1/muse1.3)
        id AA13077; Wed, 14 Dec 94 17:35:21 PST
Message-Id: <9412150135.AA13077@gaea.microunity.com>
X-Sender: tbe@gaea.microunity.com
Mime-Version: 1.0
Content-Type: text/plain; charset="us-ascii"

From: tbe@MicroUnity.com (Tom Eich)
To: sysadmin
Subject: Returned mail: unknown mailer error 1
Date: Wed, 14 Dec 94 17:35:21 PST

[Got this after filing a gnat...   -T]

>Date: Wed, 14 Dec 1994 17:33:26 -0800
>From: Mailer-Daemon@rhea (Mail Delivery Subsystem)
>Subject: Returned mail: unknown mailer error 1
>To: <tbe@gearhead>
>
>The original message was received at Wed, 14 Dec 1994 17:33:25 -0800
>from gearhead.microunity.com [192.216.193.165]
>
>   ----- The following addresses had delivery problems -----
>"|/usr/local/lib/gnats/queue-pr-q > /dev/null 2>&1" (unrecoverable error)
>   (expanded from: <gnats-dist@rhea.microunity.com>)
>
>   ----- Transcript of session follows -----
>554 "|/usr/local/lib/gnats/queue-pr-q > /dev/null 2>&1"... unknown mailer
>error 1
>
>   ----- Original message follows -----
>Return-Path: <tbe@gearhead>
>Received: from gearhead by rhea.microunity.com (8.6.4/muse-sw.2)
>   id RAA10296; Wed, 14 Dec 1994 17:33:25 -0800
>From: tbe@gearhead
>Received: by gearhead (931110.SGI.ANONFTP/930416.SGI)
>   for gnats-dist@rhea.microunity.com id AA22271; Wed, 14 Dec 94 17:31:52
>-0800
>Date: Wed, 14 Dec 94 17:31:52 -0800
>Message-Id: <9412150131.AA22271@gearhead>
>To: bugs@microunity.com
>Reply-To: tbe@gearhead
>X-Send-Pr-Version: 3.00
>
>>Submitter-Id: MUSE
>>Organization:
>MicroUnity Systems Engineering, Inc.
>>Confidential: yes
>>Severity: serious
>>Priority: medium
>>Category: PCB
>>Class: hw-bug
>>Synopsis: Smart card power connection through too-small via
>>Originator: Tom Eich
>>Release: p620-00001-0000 revision 2
>>Environment:
>Hestia main pcb
>>Description:
>An 8 mil via was used to connect Euterpe power to the smart card pin.
>
>A default via of at least 20 mil dia. should be used for manufacturing
>reasons, but the via needs to be sized based upon maximum current.
>
>Action for rev 2: Determine current and if ok proceed to test; if
>not, augment with jumper.
>
>Action for next rev: Enlarge and/or add via if necessary.
>>How-To-Repeat:

>N/A
>
>
>
>

Tom Eich | tbe@microunity.com
MicroUnity Systems Engineering, Inc.|
255 Caspian Dr. Sunnyvale, CA 94089 |
(408)734-8100, (408)734-8136 fax |

- ------- End of forwarded message -------

------- End of Forwarded Message

From:	vo (Tom Vo)
Sent:	Thursday, December 15, 1994 1:03 PM
To:	'Drew Wingard'
Cc:	'bill (William Herndon)'; 'bpw (B. P. Wong)'; 'geert (Geert Rosseel)'; 'stick (Bruce Bateman)'
Subject:	Re: Simulation conditions

```
Drew Wingard wrote ....
>
>Geert and I were thinking that if we're going to head off to do a bunch
>of simulations, we ought to make sure we can compare results easily.
>
>We therefore propose a 'standard' operating condition for simulation,
>namely stick and bpw's: 4.4V nominal CSM at 127C, i.e.
>
>* Operating Conditions for Foundry Euterpe .lib
>'/u/chip/proteus/technology/csm/hspice/models.lib' csm_60 .param
>op_temp=127 .param op_vdd=4.4
>
>.temp 'op_temp'
>vdd   vdd   vss   dc   'op_vdd'
>
>Happy Hacking,
>Drew
>
```

Just for historical perspective , this is what I'm used to seeing with previous designs .

```
10% PSU tolerance --> 4.5V
200-300mv on chip drop --> 4.2V .
```

tvo

From:	stick (Bruce Bateman)
Sent:	Thursday, December 15, 1994 1:05 PM
To:	'bill'; 'bpw'; 'geert'; 'vo'; 'wingard'
Subject:	Re: Simulation conditions

```
> Date: Thu, 15 Dec 1994 10:48:17 -0800
> From: wingard (Drew Wingard)
> To: bill, bpw, geert, stick, vo
> Subject: Simulation conditions
>
> Geert and I were thinking that if we're going to head off to do a
> bunch of simulations, we ought to make sure we can compare results easily.
>
> We therefore propose a 'standard' operating condition for simulation,
> namely stick and bpw's: 4.4V nominal CSM at 127C, i.e.
>
> * Operating Conditions for Foundry Euterpe .lib
> '/u/chip/proteus/technology/csm/hspice/models.lib' csm_60 .param
> op_temp=127 .param op_vdd=4.4
>
> .temp 'op_temp'
> vdd vdd    vss    dc     'op_vdd'
>
```

Which rail do we want to be the ground plane? Thus far in my sim's, I've actually been
setting the equivalent of:

```
.param op_vdd=-4.4v
vdd vdd 0 dc 0v
vss vss 0 dc 'op_vdd'
```

The only reason I've done this is to maintain some semblance of compatability with
netlists from euterpe/proteus/etc, thus allowing me to "borrow" netlists without having to
worry about any .param's that reference the value of 'op_vdd'. On the down-side, its
"backwards" from the way we normally think about typical CMOS circuits. I have no great
invested interest in either standard. Does anyone else have an opinion?

BB

From:	stick (Bruce Bateman)
Sent:	Thursday, December 15, 1994 1:12 PM
To:	'wingard@merope.microunity.com'; 'vo'
Cc:	'bill'; 'bpw'; 'geert'
Subject:	Re: Simulation conditions

```
> From: vo (Tom Vo)
> Subject: Re: Simulation conditions
> To: wingard@merope.microunity.com (Drew Wingard)
> Date: Thu, 15 Dec 94 11:03:07 PST
> Cc: bill (William Herndon), bpw (B. P. Wong), geert (Geert Rosseel),
>         stick (Bruce Bateman)
>
>
> Just for historical perspective , this is what I'm used to seeing with
> previous designs .
>
> 10% PSU tolerance --> 4.5V
> 200-300mv on chip drop --> 4.2V .
>
```

In memories, I've always use 100mV on chip drop, but this was for chips with ICC running
less than 100mA. We used 100mV on euterpe (3.3v - 0.3v PSU tolerance - 100mV on chip drop
= 2.9v), based primarily on the use of a space transformer. My understanding is that we
essentially plan to also use a version of a space transformer ala "micro-module" on the
CSM chip as well, albeit at higher power than on euterpe (100W?). Doesn't this imply
somewhat comparable performance for the power net?

BB

From:	vo (Tom Vo)
Sent:	Thursday, December 15, 1994 2:00 PM
To:	'bill (William Herndon)'; 'bpw (B. P. Wong)'; 'stick (Bruce Bateman)'; 'geert (Geert Rosseel)'; 'wingard (Drew Wingard)'; 'vo (Tom Vo)'; 'ong (Warren R. Ong)'; 'solo (John Campbell)'
Subject:	What's wrong with this picture

Hi ,

Here's another hand waving rectifif generating argument for those of you brave enough to consider a 500Mhz MOS level chip .

Speculate that the chip will be metal limited . Or putting it another way : we'll try to use every single available wire for interconnect if we can help it . Since 100% utilization is impossible , some TBD derating factor is needed .
This speculation stemed from the fact that every single logic chip I've worked on has been this way .

Speculate that the load due to transistors will be comparable that of the wire .

Speculate that the efficiency of a gate is 80% . As we swith the gates , not all the current goes to charging the load . Some 20% is lost in crowbar current . This figure is based on simulations done in past lives , on much older process (1.2u) .

Wish that our switching activity will be in the 30% range .
Design with many gates between latches has an easier time making this figure . I speculate that the switching rate of our shallow logic tree is closer to 100% .

Random facts .
calliope : 31.3k mm of estimated wire . 32.7k mm of actual wires as reported by GARDS .
Note that the GARDS number does not include wires used to route the internal of a cell .
geert_euterpe : 42k mm of estimated wire for an incomplete euterpe
placement .

With a 500k atoms baseplate , the available wires per layer is 48k mm We try to use little of M2 in GARDS routing so if we guess that a fully routed euterpe is some 50k mm of wires , most of that in M3/M4 , we use
some 50% of the M3/M4 wiring available .

Trying to extrapolate to how much wires we'll use in a CSM size die , I increase the usage to 75% (more custom layout) , and guess 11x16mm as a size for the logic area . Using a 2.4u routing pitch , the available wires per layer is 74k mm . With these guesses , I speculate that the total wires we'll use is 111k mm .

Using a .3pf/mm of wire , 111k mm --> 33.3nF At 500Mhz , and 5V supply , the CVF current for 33.3nF is 83 Amps Apply 80% gates efficiency , 83 Amps --> 100 Amps just to swing 2 layers of wires .
Add transistor load , 100 Amps --> 200 Amps Apply the wished for 30% switching activity , 200 Amps --> 60 Amps .

So , neglecting the wires used in the routing of the cell internals , all the memories , and shooting for a 30% switching activity , we're looking at a 300W chip .

tvo

From: woody (Jay Tomlinson)

Sent: Thursday, December 15, 1994 4:02 PM

To: 'jeffm (Jeff Marr)'

Cc: 'djc'; 'tbr'; 'brian'

Subject: forwarded message from Dave Conroy

Jeff Marr wrote (on Thu Dec 15):
------- Start of forwarded message -------
Status: RO
X-VM-v5-Data: ([nil nil nil] nil nil nil nil nil nil]
    [nil nil nil nil nil nil nil nil nil nil nil nil "^From:" nil nil nil])
Return-Path: <djc>
Received: from boreas.microunity.com by gaea.microunity.com (4.1/muse1.3)
    id AA08381; Thu, 15 Dec 94 13:10:08 PST
Received: from localhost by boreas.microunity.com (8.6.4/muse-sw.3)
    id NAA07520; Thu, 15 Dec 1994 13:10:21 -0800
Message-Id: <199412152110.NAA07520@boreas.microunity.com>
From: djc (Dave Conroy)
To: jeffm
Subject: Re: gtlbda
Date: Thu, 15 Dec 1994 13:10:21 -0800

> From jeffm Thu Dec 15 12:54:38 1994
> Date: Thu, 15 Dec 1994 12:54:45 -0800
> From: jeffm (Jeff Marr)
> To: lisar
> Cc: djc, billz
> Subject: gtlbda
> Content-Length: 435
>
> Well ......
>
> The problem that shows up in the vlog is that the hermes channels
> are being inadvertantly turned on. At the point when the second
> store to the gtlb happens, the prb's from both hermes channels
> go to X. This is a bit of a latency, so it just comes out of the
> blue. The X's ripples though, causing acute discomfort.
>
> I will fix and rerun in zycad. This same problem should apply to
> all the gtlbXX tests.
>
> Thanx,
>
> jeffm
>
The tests don't explicitly disable the hermes channels when the cerb oct 6
is written to enable memory management but should that really cause a
problem? Is this an artifact to the test environment or a real problem?
If a real problem, should it have been caught by terp?
------- End of forwarded message -------
What will happen, when we have real HW, if a Hermes channel gets enabled
when there is no device on that channel?

Thanx,

jeffm

Just what happened. din/clkin. When the channel is enabled (plus a delay for
the rate fifo to synchronize), the input packets will be interpreted. If the
'header' is X, then the prb will get corrupted as you saw. You will also
potentially get X's in the Event Register.

Jay

From:	wingard (Drew Wingard)
Sent:	Thursday, December 15, 1994 4:56 PM
To:	'bill'; 'bpw'; 'geert'; 'ong'; 'solo'; 'stick'; 'vo'
Subject:	Re: What's wrong with this picture

Tom Vo sez:
<snip>
> So , neglecting the wires used in the routing of the cell internals ,
> all the memories , and shooting for a 30% switching activity , we're
looking at
> a 300W chip .

Ouch. That sounds really bad. Let me get out my slingshot, and see if I can bring this
giant down to size...

<snip>
> With a 500k atoms baseplate , the available wires per layer is 48k mm
> We try to use little of M2 in GARDS routing so if we guess that a
> fully routed euterpe is some 50k mm of wires , most of that in M3/M4 , we use
> some 50% of the M3/M4 wiring available .
>
> Trying to extrapolate to how much wires we'll use in a CSM size die ,
> I increase the usage to 75% (more custom layout) , and guess 11x16mm
> as a size for the logic area . Using a 2.4u routing pitch , the
> available wires per layer is 74k mm . With these guesses , I
> speculate that the total wires we'll use is 111k mm .

Hmm. One assumption we've made is that Mobi is roughly four times as dense as other .5um
processes. If we're truly wire limited, and the wire pitch ratio is 2.4/1, then I'd claim
the CSM design might be 2.4x in each dimension.
However, we're planning to go to single-ended signalling rather than differential.
There is a (peak) factor of 2 in our favor (ratio 1/2) in each linear dimension. We use
some single-ended stuff already, so maybe the right ratio is (1/1.7). I'll bet it
wouldn't be that difficult to come up with the 'right' number out of geert_euterpe.

So, again assuming that we're truly wire limited, I don't see why our total wire length
should go up any more that $(2.4/1.7)**2 == 1.99$. Furthermore, custom design should
reduce the total wire length by increasing the usage and thus reducing the required
area. I claim that at least half of Euterpe would be subject to custom design, and if we
can achieve the maximum routing density offered by the process (2.0um pitch) in the custom
areas, then the wire length ratio would be more like
$.5*[(2.4/1.7)**2 + (2/1.7)**2] == 1.68$.

This implies that the Euterpe wire length would grow to (50k mm)*(1.68) == 85k mm.

<snip>
> Speculate that the efficiency of a gate is 80% . As we swith the
> gates , not all the current goes to charging the load . Some 20% is
> lost in crowbar current . This figure is based on simulations done in
> past lives , on much older process (1.2u) .

Isn't this more true of static CMOS than precharge/discharge circuits? I thought that the
delay to the second discharge stage in a domino chain allowed the precharge transistor to
turn off before any inputs get a chance to evaluate. Not that precharge discharge doesn't
have its own power problems...

<snip>
> Wish that our switching activity will be in the 30% range .
> Design with many gates between latches has an easier time making this
> figure . I speculate that the switching rate of our shallow logic
> tree is closer to 100% .

I think that this is a very important point. We've been saying that we need to try to
reduce the number of transitions. If we use traditional precharge-discharge everywhere,

we know that we generate lots of spurious transitions - in the worst case, our wires make
two transitions per cycle (just like the 500MHz clock). That's 100% switching activity.
Our OR structures (probabilistically speaking) asymptotically approach this limit as their
fanin increases.

I strongly believe that we cannot afford this. Thus my argument for some sort of latch
discipline that reduces the maximum number of transitions on a wire to one per *cycle*
(50% peak switching activity). If we say that the probability of any given output being
different on any two cycles is 50% (and I'll bet that the real answer is lower than that),
we're down to 25% realistic switching rate.

<snip>
> Using a .3pf/mm of wire , 111k mm --> 33.3nF At 500Mhz , and 5V supply
> , the CVF current for 33.3nF is 83 Amps Apply 80% gates efficiency ,
> 83 Amps --> 100 Amps just to swing 2 layers of wires .
> Add transistor load , 100 Amps --> 200 Amps Apply the wished for 30%
> switching activity , 200 Amps --> 60 Amps .

So, if I follow this formula:
85k mm wire * .3pF/mm -> 25.5nF
Ipeak @ 500MHz, 5V == (25.5nF)*(5V)/2ns -> 64A 80% gate efficiency: (64/.8) -> 80A Double
for transistor load: -> 160A 25% switching activity: -> 40A

So that's 200W. Which is still too much. But, I wonder how conservative the 25%
switching and the transistor load == wire load assumptions are?

If we take the SOFA area of Euterpe (500k atoms * 96um^2/atom == 48mm^2) and multiply it
by our (wire-limited) area ratio of 1.68, we get a CSM logic area of about 80mm^2. If we
assume that we fully populate this area with a CSM "atom" containing an NMOS and a PMOS
device, fully isolated, with 5um gate widths each, we need an atom area of (4.8um x 15.6um
==) 75um^2.
We end up with approximately (10um*(80mm^2/75um^2) ==) 10 *meters* of channel width. If
we could hook up each of these to a wire (we can't), the total transistor switching
capacitance would be
(10e6 um * .6um * 2.6fF/um^2 ==) 16.6nF. So, it seems to me like the equal transistor and
wire capacitance is a bit pessimistic.

I claim a more realistic, but still conservative, estimate would be more like 175W. And
this is without considering the effect of blocks (such as the Hermes controllers) that
spend considerable time idle, and ignore microarchitectural and circuit changes
(redesigning NB, etc to run at half rate, gating clocks to idle datapath units, etc) that
can drastically cut down the switching activity.

I believe that power dissipation is our #1 concern (with clocks close behind, and closely-
related). But I don't think the sky is falling yet...

Drew

From: vo (Tom Vo)
Sent: Thursday, December 15, 1994 5:47 PM
To: 'Drew Wingard'
Cc: 'bill (William Herndon)'; 'bpw (B. P. Wong)'; 'geert (Geert Rosseel)'; 'ong (Warren R. Ong)'; 'solo (John Campbell)'; 'stick (Bruce Bateman)'
Subject: Re: What's wrong with this picture

Drew Wingard wrote ....
>
><snip>
>> Speculate that the efficiency of a gate is 80% . As we swith the
>> gates , not all the current goes to charging the load . Some 20% is
>> lost in crowbar current . This figure is based on simulations done
>> in past lives , on much older process (1.2u) .
>
>Isn't this more true of static CMOS than precharge/discharge circuits?
>I thought that the delay to the second discharge stage in a domino
>chain allowed the precharge transistor to turn off before any inputs
>get a
chance
>to evaluate. Not that precharge discharge doesn't have its own power
>problems...

Yes . But I can't believe that we're not going to have static gates .
And as you pointed out , generating spurious transitions with precharge/discharge circuits
is not going make it any better .

><snip>
>If we take the SOFA area of Euterpe (500k atoms * 96um^2/atom ==
>48mm^2) and multiply it by our (wire-limited) area ratio of 1.68, we
>get a CSM logic area of about 80mm^2. If we assume that we fully
>populate this
area
>with a CSM "atom" containing an NMOS and a PMOS device, fully isolated,
with
>5um gate widths each, we need an atom area of (4.8um x 15.6um ==) 75um^2.
>We end up with approximately (10um*(80mm^2/75um^2) ==) 10 *meters* of
>channel width. If we could hook up each of these to a wire (we can't),
>the total transistor switching capacitance would be
>(10e6 um * .6um * 2.6fF/um^2 ==) 16.6nF. So, it seems to me like the
>equal transistor and wire capacitance is a bit pessimistic.

80mm^2 is 28% of 17x17mm chip .   We need to add more functionality :-)

>
>I claim a more realistic, but still conservative, estimate would be
>more like 175W. And this is without considering the effect of blocks
>(such as the Hermes controllers) that spend considerable time idle, and
>ignore microarchitectural and circuit changes (redesigning NB, etc to
>run at
half
>rate, gating clocks to idle datapath units, etc) that can drastically
>cut down the switching activity.

Add the ignored M1 layer and the missing memories to this giant and things look scary
again .

We really need a tool to monitor switching activities .
Got to look out for those applications requiring all 5 cyclinders to run for sustained
periods .

tvo

------- Start of forwarded message -------
Return-Path: <Mailer-Daemon>
Received: from aphrodite.microunity.com by gaea.microunity.com
(4.1/muse1.3)
        id AA01485; Thu, 15 Dec 94 07:11:38 PST
Received: from localhost by aphrodite.microunity.com (8.6.4/muse-sw.3)
        id JAB01273; Thu, 15 Dec 1994 09:27:10 -0800
Message-Id: <199412151727.JAB01273@aphrodite.microunity.com>
From: Mailer-Daemon (Mail Delivery Subsystem)
Apparently-To: <tbr@gaea>
Subject: Returned mail: User unknown
Date: Thu, 15 Dec 1994 09:27:10 -0800

The original message was received at Thu, 15 Dec 1994 09:27:10 -0800 from tbr@localhost

    ----- The following addresses had delivery problems ----- geeert   (unrecoverable error)

    ----- Transcript of session follows ----- 550 geeert... User unknown

        ----- Original message follows -----
Return-Path: <tbr>
Received: from localhost by aphrodite.microunity.com (8.6.4/muse-sw.3)
        id JAA01273; Thu, 15 Dec 1994 09:27:10 -0800
Date: Thu, 15 Dec 1994 09:27:10 -0800
From: tbr (Tim B. Robinson)
Message-Id: <199412151727.JAA01273@aphrodite.microunity.com>
To: mws (Mark Semmelmeyer)
Cc: billz (Bill Zuravleff), dickson (Richard Dickson), geeert,
        woody@MicroUnity.com (Jay Tomlinson)
Subject: Re: Euterpe top-level
In-Reply-To: <199412150746.XAA10980@clytemnestra.microunity.com>
References: <199412150544.VAA14654@orion.microunity.com>
        <199412150746.XAA10980@clytemnestra.microunity.com>

Mark Semmelmeyer wrote (on Wed Dec 14):

    woody wrote:

    > ... this is an hr->muxen->muxen-hr path to sr. In fact
    > (somebody correct me if I am wrong) I think these
    > could be 2s since the data is loaded into the hr and
    > re-circulates (mux-hr) for a lot of cycles before it is actually used by sr.

    I think we should be very sure we want to violate timing on logic paths.
    Normal usage would allow lots of cycles for the data to transmit,
    but software is still free to read the fva at any time. To keep
    such reads on architecturally visible paths deterministic, we would
    have to limit the paths to two ticks.

I agree. It's already scary that we have multicycle paths in the arrays and we are
building special models to detect algorithmic violations there. Let's not create more
except in absolute desperation!

    > phys address (Upa4700R12/u47:0) as 24s. This is currently a
ff->muxff path to
    > cc, it could be an hr->mux->hr path if cc is allowed to use the 1st-cycle of
    > the two.

If cc is allowed to use the 1st cycle, then it is a one tick path
and hr --> whatever --> hr does not help (in fact I believe gloss
will flag it as a phase error).

There was a case I think where addition of buffers allowed one path to be single cycle and
another double cycle with a net saving because the double path was really easy (buffer
goes in that path of course). Is this one amneable to similar treatment?

Tim

------- End of forwarded message -------

From:	tbr
Sent:	Thursday, December 15, 1994 9:42 PM
To:	'lisar (Lisa Robinson)'
Cc:	'bobm'; 'euterpe'; 'jeffm'; 'veena'
Subject:	e-shift overflow
Follow Up Flag:	Follow up
Flag Status:	Red

Lisa Robinson wrote (on Thu Dec 15):

 I still haven't seen any mail describing the behavior of these
 instructions.

Checking the records there have been several messages, though not
correct :-)

We decided some time back that since we were not supporting these per
the spec they should cause illegal instruction traps rather than
simply ignore the overflow. That way it is at least possible to
emulate the behavior of the full architecture. I believe this is also
the behavior of the instruction level simulator.

Tim

From: tbr (Tim B. Robinson)
Sent: Thursday, December 15, 1994 9:42 PM
To: 'lisar (Lisa Robinson)'
Cc: 'bobm'; 'euterpe'; 'jeffm'; 'veena'
Subject: e-shift overflow

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> instructions.

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cause illegal instruction traps rather than simply ignore the overflow. That way it is at
least possible to emulate the behavior of the full architecture. I believe this is also
the behavior of the instruction level simulator.

Tim

From: tbr

Sent: Thursday, December 15, 1994 9:49 PM

To: 'dickson (Richard Dickson)'

Subject: euterpe/verilog/bsrc/es es.V es.power.tab.top

Follow Up Flag: Follow up

Flag Status: Red

Richard Dickson wrote (on Thu Dec 15):

Update of /p/cvsroot/euterpe/verilog/bsrc/es
In directory staypuft:/N/rama/root/s5/dickson/euterpe/verilog/bsrc/es

Modified Files:
es.V es.power.tab.top
Log Message:
powered down hr's that drive lva.
also make lva bus 64 bits at interface.
upper 64 bits go nowhere and should get
pruned.

If they go to the interface they won't because they end up in the
power.tab.local file in dontprune statements.

From:	tbr (Tim B. Robinson)
Sent:	Thursday, December 15, 1994 10:04 PM
To:	'mws (Mark Semmelmeyer)'
Cc:	'bobm'; 'euterpe'; 'jeffm'; 'lisar'; 'veena'
Subject:	Re: e-shift overflow

Mark Semmelmeyer wrote (on Thu Dec 15):

> From tbr Thu Dec 15 18:46:56 1994

> We decided some time back that since we were not supporting these per
> the spec they should cause illegal instruction traps rather than
> simply ignore the overflow.

>From the cvs log of bsrc/BOM:

revision 177.0
date: 1994/11/16 13:26:21 LT;   author: mws;   state: Exp;   lines: +1 -1
Release Target: euterpe/verilog/bsrc

. . .
opchart: Change EShLO EShLUO EShLIO EShLIUO overflow shifts to reserved xcptn.
. . .

Thanks. The issue was entirely one of documentation I think . . .

Tim

latest results in /n/ghidra/s4/vo/lisar/euterpe/verilog/bsrc/xlu

From: hopper (Mark Hofmann)
Sent: Friday, December 16, 1994 7:26 AM
To: 'Geert Rosseel'
Cc: 'wampler (Kurt Wampler)'; 'brianl (Brian Lee)'; 'tbr (Tim B. Robinson)'; 'tom (Thomas Laidig)'; 'vo (Tom Vo)'
Subject: Re: problem in /u/chip .. URGENT

Geert Rosseel writes:
    Hi,

    I don't know who owns this , but the make of /u/chip/euterpe/verilog/bsrc/uu failed
    because of :

    ###Creating uu-pass3.ly
    (Compacting...done)
        Parsing translation table
/n/auspex/s10/chip/euterpe/tools/lib/gards/xlatemobi.tab
        Design uu-pass3   Created 00/00/00 Gil Version 1   Gil Level
2
        Number of records processed: 94993
        Write layout files
    ###Abstracting leaf cell outlines as placement obstructions
    /bin/nawk: input record `# "16-Dec-94 GMT" "2...' too long
     input record number 1
     source line number 3
    gmake[2]: *** [gards/uu-pass3.obs] Error 2

My first thought:

    use /usr/local/bin/gawk

    -hopper

Mark Semmelmeyer wrote (on Thu Dec 15):

> From tbr Thu Dec 15 18:46:56 1994

> We decided some time back that since we were not supporting these per
> the spec they should cause illegal instruction traps rather than
> simply ignore the overflow.

>From the cvs log of bsrc/BOM:

revision 177.0
date: 1994/11/16 13:26:21 LT;   author: mws;   state: Exp;   lines: +1 -1
Release Target: euterpe/verilog/bsrc

...
opchart: Change EShLO EShLUO EShLIO EShLIUO overflow shifts to reserved xcptn.
...

Thanks.

I will remove the following tests from the regression template.

dpeshliospc_0
dpeshliuospc_0
dpeshluospc_0
dpeshlospc_0

Veena, Jeff

Are they covered in the exception tests.

Lisa R.

From:	tbr
Sent:	Friday, December 16, 1994 11:00 AM
To:	'lisar (Lisa Robinson)'
Cc:	'doi'
Subject:	** compv
Follow Up Flag:	Follow up
Flag Status:	Red

Lisa Robinson wrote (on Fri Dec 16):

Tim I noticed ...

ERROR: Cell if is not found in any library.
ERROR: Cell if is not found in any library.
ERROR: Cell rgrfwstbwm is not found in any library.
ERROR: Cell if is not found in any library.
ERROR: Cell if is not found in any library.
ERROR: Cell rginc8 is not found in any library.
ERROR: Cell rgpcinc is not found in any library.
ERROR: Cell if is not found in any library.
ERROR: Cell rginc8 is not found in any library.
ERROR: Cell rgpcinc is not found in any library.
ERROR: Cell if is not found in any library.
ERROR: Cell if is not found in any library.
ERROR: Cell rgrfwstbwm is not found in any library.
ERROR: Cell if is not found in any library.
ERROR: Cell */ is not found in any library.
ERROR: Cell if is not found in any library.
ERROR: Cell unix. is not found in any library.

Is this OK?

Seem makerrs on /n/rhodan/s3/euterpe/verilog/bsrc.

Seems not to be causing a problem (if it did you would either be
missing a module from the list, or would have a bogus one it could not
find).

vltree needs work, but if ikos keep promising a vlit that knows how to
search libraries the requirement might go away.

Tim

From: solo (John Campbell)

Sent: Friday, December 16, 1994 11:04 AM

To: 'Lisa Robinson'

Cc: 'mudge (john mudge)'; 'wayne (Wayne Freitas)'; 'tbr (Tim B. Robinson)'

Subject: Re: Static damage

as Lisa Robinson was saying ....

..

..

..John Campbell wrote (on Fri Dec 16):

..

.. as Lisa Robinson was saying ....

.. ..

.. ..

.. ..John,

.. ..

.. ..How goes the thoughts on a Static Damage "Seminar". I'd really like

.. ..folks to have the opportunity to be educated before the main board

.. ..comes in.

.. ..Perhaps we could arrange it to be repeated every 3 -6 months, and a

.. ..handout to all new employees.

.. ..

.. ..

.. ..Lisa R.

.. ..

.. I have talked to mudge and we have committed to make a committment.

.. he agrees on the importance of it. i think between he and i, we may

.. have enough to at least grab knowledge that we don't have.

..

.. maybe i should get a date when the board is expected and that would

.. motivate us to get going.

..

.. i think only you have that knowledge among the three of us.

..

..That's great.

..

..Then next week would in line! How about Thursday.

..

..Lisa R.

..

..

sounds agressive but i will talk to mudge about an outline and maybe

it could happen. no promises. you didn't say when we will be

stuffing euterpes into the board.

....

regards,

solo a.k.a. John Campbell   x516

From: lisar (Lisa Robinson)

Sent: Friday, December 16, 1994 11:32 AM

To: 'jeffm'; 'veena'

Cc: 'tbr'

Subject: Ikos different

I have been running all of the datapath tests against BOM 187 on the
IKOS. I have found that a few datapath tests fail on the IKOS where
they don't on the zycad.
Could you look at the traces

/n/nosferatu/s2/euterpe/verilopg/bsrc/res/161294.20327/results/dpemshrspc_0.dpo

and

/n/rhodan/s4/euterpe/verilog/bsrc/res/rundp/results/dpemshrspc_0.dpo

They differ quite early in the test (zycad simtick 61160). I am
running the same binaries on both. NOTE in the zycad trace the
"commit" signal is one cycle earlier than in the IKOS trace this is
because there is no advantage in tracing a higher level signal on the
IKOS).

Lisa R.

This is the list of the tests which fail on the IKOS which I was
expecting to run ok. (I am re-running on the zycad at the moment)

        Design Name: z_euterpe_wrap
        Run Date: 161294
        Run ID: 20327

Simulator: z_euterpe_wrap.mif.mm was built on Fri Dec 2 7:21:06 1994

Using BOM: Version BOM,v 187.0-R1 1994/12/01 22:06:20 LT woody
Warning: Local BOM is out of date ...
Latest BOM is: RCS Version: 194.0 /p/cvsroot/euterpe/verilog/bsrc/BOM,v
Warning: Local BOM differs from that used to build z_euterpe_wrap.mif.mm
Created by mkbom
$Id: BOM,v 193.0 1994/12/15 01:37:52 LT mws Exp $

Log Message:
Run started on host: nosferatu at: Fri Dec 16 06:55:38 PST 1994

        dpexlushort_0   Ran ok
Run time = 676.5 seconds Performance = 14 cycles/second
        dpgxlushort_0   Ran ok
Run time = 667.7 seconds Performance = 14 cycles/second

```
        dpemshrspc_0    Ran ok
Run time = 2471 seconds Performance = 13 cycles/second
        dpemshrispc_0    Ran ok
Run time = 2169 seconds Performance = 13 cycles/second
        dpemdepispc_0    Queued .. No result
        dpgmdepispc_0    Queued .. No result
      dpgmshrspc128_0    Queued .. No result
       dpgmshrspc64_0    Queued .. No result
     dpgmshrispc128_0    Queued .. No result
      dpgmshrispc64_0    Queued .. No result
      dpgmshrispc32_0    Queued .. No result
      dpgmshrispc16_0    Queued .. No result
       dpgmshrispc8_0    Queued .. No result
       dpgmshrispc4_0    Queued .. No result
       dpgmshrispc2_0    Queued .. No result


--------------------------------------------------------------------
```

From: lisar (Lisa Robinson)

Sent: Friday, December 16, 1994 11:34 AM

To: 'tbr'

Cc: 'dickson'

Subject: *** Compv

BOM 194

Pass = 2
Top level modules:
 i_euterpe_wrap
Pass2: Module es has 62 ports, instance es has 64 ports
Instance es has more ports than its module
Line = 1411, char = 12
!!!! Semantic error

Lisa R.

From: paulb (Paul Berry)
Sent: Friday, December 16, 1994 12:02 PM
To: 'craig'
Subject: pandora viewgraphs

Could I include in the notes the content of the foils you showed at the Pandora meeting
yesterday? Could you point me to the file they're in?

hi kurt,

IFE, which routed easily before, routed even easier with the new routing strategy. it used to converge in 2 iterations. this time it converged in pass3. i notice from my log file (you can look in ~hopper/chip/euterpe/verilog/bsrc/ife/out) that some maze routing was performed for 1 or 2 wires on a pass.

I'm running a more substantial test, NB, and will let you know the results of that when it completes.

-hopper

From: lisar (Lisa Robinson)

Sent: Friday, December 16, 1994 1:54 PM

To: 'tbr'

Subject: z redefined

is this okay

```
gmake[1]: Leaving directory `/N/aphrodite/root/s3/euterpe/verilog/bsrc/au'
gmake[1]: Entering directory `/N/aphrodite/root/s3/euterpe/verilog/bsrc/cc'
cat /n/aphrodite/s3/euterpe/proteus/verilog/diff.h cc.V | /lib/cpp  -P -C -B | sed -e '/^$/d'> cc.v.tmp
376: z redefined
377: z_N redefined
380: z redefined
381: z_N redefined
mv cc.v.tmp cc.v
```

Lisa R.

From: geert (Geert Rosseel)

Sent: Friday, December 16, 1994 3:23 PM

To: 'wampler'

Cc: 'brianl'; 'hopper'; 'tbr'; 'tom'; 'vo'

Subject: problem in /u/chip .. URGENT

Hi,

I don't know who owns this , but the make of /u/chip/euterpe/verilog/bsrc/uu failed
because of :

```
###Creating uu-pass3.ly
(Compacting...done)
    Parsing translation table /n/auspex/s10/chip/euterpe/tools/lib/gards/xlatemobi.tab
        Design uu-pass3 Created 00/00/00        Gil Version 1   Gil Level 2
        Number of records processed: 94993
    Write layout files
###Abstracting leaf cell outlines as placement obstructions
/bin/nawk: input record `# "16-Dec-94 GMT" "2...' too long
 input record number 1
 source line number 3
gmake[2]: *** [gards/uu-pass3.obs] Error 2
```


                    Geert

From: hopper (Mark Hofmann)

Sent: Friday, December 16, 1994 3:32 PM

To: 'tom (Thomas Laidig)'; 'wampler (Kurt Wampler)'; 'vant'

Cc: 'solo (John Campbell)'; 'tbr (Tim B. Robinson)'

Subject: Re: VerifyRun snap (fwd)

Tim B. Robinson writes:
New touble:

```
done
### finished making dependencies -- Fri Dec 16 21:02:43 PST 1994
gmake[1]: Leaving directory `/N/auspex/root/s23/euterpe-proteus-cp/gards'
gmake[1]: Entering directory `/N/auspex/root/s23/euterpe-proteus-cp/gards'
gmake[1]: *** No rule to make target `_MISSING_LAYOUT_FILE_'.
gmake[1]: *** No rule to make target `scxbcgdr1.ly'.
### making sofa/ealporl6nf8s3x4a.pdl -- Fri Dec 16 21:03:07 PST 1994
HOME=/n/auspex/s23/euterpe-proteus-cp/tools CHIPROOT=/n/auspex/s23/euterpe-proteus-cp /n/auspex/s23/euterpe-
proteus-cp/tools/bin/piddles -x 'vrr\[.\]' -x vii -r -t mobi234 -c via12 -x vsse -x vdde -x vdda -x vssa -x vcca -g vssc=vssc -g
vddc=vddc -g phi_a  2p_glob=phi_a2p -g phi_b2p_glob=phi_b2p -g phim_a1p_glob=phim_a1p -g
phim_b1p_glob=phim_b1p -g vref_0ph_glob=vref_0ph -v /n/auspex/s23/euterpe-proteus-cp/compass/vlsi.boo-all -V
vlsimm_script ealporl6nf8s3x4a > sofa/ealporl6nf8s3x4a.pdl.tmp
  Translation of /usr/tmp/piddles18677/ealporl6nf8s3x4a.cif succeeded.
  Root symbol is called ROOTCELL.
  G
  .
  .


Elapsed wall clock time :  0 Hrs   0 Mins   0 Secs
  CHIPROOT=/n/auspex/s23/euterpe-proteus-cp /n/auspex/s23/euterpe-proteus-cp/proteus/gards/basegen/derive_cutouts -
v /n/auspex/s23/euterpe-proteus-cp/compass/vlsi.boo-all -c ealporl8nf8s3x4a -o sofa//ealporl8nf8s3x4a.cutouts
  mv sofa/ealporl8nf8s3x4a.pdl.tmp sofa/ealporl8nf8s3x4a.pdl
  ### finished with sofa/ealporl8nf8s3x4a.pdl -- Fri Dec 16 21:03:54 PST 1994
  gmake[1]: Target `sofapdls' not remade because of errors.
```

Hmmm... This seems to be a complaint about scxbcgdr1.ly. That's a new
cell to me. Is there layout that needs to be checked in, does anyone know?

 thanks,
-hopper

From: hopper (Mark Hofmann)

Sent: Friday, December 16, 1994 3:33 PM

To: 'Tim B. Robinson'

Cc: 'wampler (Kurt Wampler)'; 'solo (John Campbell)'

Subject: Re: Is this a problem

Tim B. Robinson writes:

```
make[2]: Entering directory `/N/auspex/root/s23/euterpe-proteus-cp/gardswarts/pl_eus_logic'
Makefile:43: warning: overriding commands for target `pl_eus_logic.spn'
/n/auspex/s23/euterpe-proteus-cp/gardswarts/protowart/Makefile.opt:201: warning: ignoring old commands for target
`pl_eus_logic.spn'
Makefile:51: warning: overriding commands for target `pl_eus_logic.emerge.tab'
/n/auspex/s23/euterpe-proteus-cp/gardswarts/protowart/Makefile.opt:102: warning: ignoring old commands for target
`pl_eus_logic.emerge.tab'
Makefile:75: warning: overriding commands for target `pl_eus_logic.rcf'
/n/auspex/s23/euterpe-proteus-cp/gardswarts/protowart/Makefile.opt:193: warning: ignoring old commands for target
`pl_eus_logic.rcf'
gmake[2]: Nothing to be done for `default'.
gmake[2]: Leaving directory `/N/auspex/root/s23/euterpe-proteus-cp/gardswarts/pl_eus_logic'
gmake  -C pl_euh_logic
gmake[2]: Entering directory `/N/auspex/root/s23/euterpe-proteus-cp/gardswarts/pl_euh_logic'
Makefile:43: warning: overriding commands for target `pl_euh_logic.spn'
/n/auspex/s23/euterpe-proteus-cp/gardswarts/protowart/Makefile.opt:201: warning: ignoring old commands for target
`pl_euh_logic.spn'
Makefile:51: warning: overriding commands for target `pl_euh_logic.emerge.tab'
/n/auspex/s23/euterpe-proteus-cp/gardswarts/protowart/Makefile.opt:102: warning: ignoring old commands for target
`pl_euh_logic.emerge.tab'
Makefile:74: warning: overriding commands for target `pl_euh_logic.rcf'
/n/auspex/s23/euterpe-proteus-cp/gardswarts/protowart/Makefile.opt:193: warning: ignoring old commands for target
`pl_euh_logic.rcf'
```

I don't _think_ so, but Kurt or Tom are in a much better position to call
this one.

-hopper

From:	wampler (Kurt Wampler)
Sent:	Friday, December 16, 1994 3:52 PM
To:	'geert'
Cc:	'brianl'; 'hopper'; 'tbr'; 'tom'; 'vo'
Subject:	Re: problem in /u/chip .. URGENT

```
Geert writes:
------------
> I don't know who owns this , but the make of
/u/chip/euterpe/verilog/bsrc/uu failed
>because of :
>
>###Creating uu-pass3.ly
>(Compacting...done)
>     Parsing translation table
/n/auspex/s10/chip/euterpe/tools/lib/gards/xlatemobi.tab
>     Design uu-pass3   Created 00/00/00  Gil Version 1     Gil Level
2
>      Number of records processed: 94993
>     Write layout files
>###Abstracting leaf cell outlines as placement obstructions
>/bin/nawk: input record `# "16-Dec-94 GMT" "2...' too long  input
>record number 1  source line number 3
>gmake[2]: *** [gards/uu-pass3.obs] Error 2
```

   The problem was in the export_obs script; nawk was unable to handle the
   subcells line in the Compass file that was being generated. At Hopper's
   suggestion it has been changed to gawk. I've releasebom'ed a new version
   of this euterpe/verilog/bsrc/export_obs script -- it *should* fix the
   problem.

   - Kurt

Buffalo Chip wrote (on Fri Dec 16):
    The output from euterpe/verilog/bsrc/uu/.checkoutrc is 408k, so it is not included
    in this mail message. Instead, check the file

    /n/tmp/chiplog/woody.godzilla.26981.euterpe-verilog-bsrc-uu

    (which is accessible from all machines). This file will disappear in
    about 5 days.

    By the way, the exit status returned by .checkoutrc was 1.

geert,

UU got this error again(extracted from /u/chip.../uu/gards/makerrs). It looks like a
Makefile problem. Any idea where it came from?
Jay

Elapsed wall clock time : 0 Hrs   0 Mins 42 Secs
###Creating uu-pass3.ly
(Compacting...done)
    Parsing translation table
/n/auspex/s10/chip/euterpe/tools/lib/gards/xlatemobi.tab
    Design uu-pass3   Created 00/00/00 Gil Version 1   Gil Level
2
    Number of records processed: 94993
    Write layout files
###Abstracting leaf cell outlines as placement obstructions
/bin/nawk: input record `# "16-Dec-94 GMT" "2...' too long input record number 1 source
line number 3
gmake[2]: *** [gards/uu-pass3.obs] Error 2
gmake[2]: Leaving directory
`/N/auspex/root/s10/chip/euterpe/verilog/bsrc/uu'
gmake[1]: *** [uu-base.netcap] Error 1
rm uuruptr12.esp uuchkdstuw.optesp uuprblmr0.optesp uuthruut.optesp uustepuu.optesp
uuprblmup.optesp uursltbypbuu.optesp uuchkdstr3.optesp uubruw.optesp uurstuq.esp
uusteput.optesp uuprblmr10.optesp uuholduu.optesp uuprblmr8.optesp uurbuu.optesp
uuprblmr7.optesp uupreemuq.optesp uursltbypcuu.optesp uurbuu.esp uursltbypauu.esp
uuprblmwm.optesp uuprblmfrz.optesp uuprblmr11.optesp uuprblmr5.optesp uupreemuq.esp
uujoblstux.optesp uuprblmr9.optesp uuprblmr13.optesp uujoblstux.esp uuprblmr12.optesp
uursltbypauu.optesp uursltbypbuu.esp uurstuq.optesp uuwewj.optesp uuruptr12.optesp
gmake[1]: Leaving directory
`/N/auspex/root/s10/chip/euterpe/verilog/bsrc/uu'
gmake: *** [uugards] Error 1

From: lisar (Lisa Robinson)

Sent: Friday, December 16, 1994 4:31 PM

To: 'tbr'

Subject: forwarded message from Jeff Marr

------- Start of forwarded message -------
Status: RO
X-VM-v5-Data: ([nil nil nil nil nil nil nil nil nil]
     ["381" "Fri" "16" "December" "1994" "14:29:09" "-0800" "Jeff Marr" "jeffm " nil "8" "SDRAM c model" "^From:" nil
nil "12"])
Return-Path: <jeffm>
Received: from thalia.microunity.com by gaea.microunity.com (4.1/muse1.3)
     id AA05898; Fri, 16 Dec 94 11:07:00 PST
Received: from localhost by thalia.microunity.com (8.6.4/muse-sw.3)
     id OAA11017; Fri, 16 Dec 1994 14:29:09 -0800
Message-Id: <199412162229.OAA11017@thalia.microunity.com>
From: jeffm (Jeff Marr)
To: lisar
Subject: SDRAM c model
Date: Fri, 16 Dec 1994 14:29:09 -0800

What I sent you yesterday is about how it has to be done, per Pat.
I currently can only attach a C model to signals that come out of the
toplevel euterpe_wrap port. Currently this includes only poko,rdata,
and strobe. With the current state of the IKOS tools, I have to bring
the dram interface out thru the wrapper - I cannot instantiate the sdram
c model in the verilog.

jeffm
------- End of forwarded message -------

From: woody (Jay Tomlinson)

Sent: Friday, December 16, 1994 5:47 PM

To: 'lisar'; 'jeffm'

Cc: 'tbr'; 'mws'; 'dickson'

Subject: test1 status

test1 ran to fab on BOM 194. I used wraprsbim. I modified Makefile and euterpe_wrap.V so that I could pass RSTPCIBUF through the Makefile. I only modified r_euterpe_wrap.v target.

Jay

From: woody (Jay Tomlinson)

Sent: Friday, December 16, 1994 5:55 PM

To: 'mws (Mark Semmelmeyer)'

Cc: 'lisar'; 'jeffm'; 'tbr'; 'dickson'

Subject: Re: test1 status

Oops. yes I meant wraprsim.
Mark Semmelmeyer wrote (on Fri Dec 16):
> test1 ran to fab on BOM 194. I used wraprsbim. I modified Makefile and
Do you mena wraprsim? ----------------^^^^^^^^^^
I was able to find the other terms you mention.

> euterpe_wrap.V so that I could pass RSTPCIBUF through the Makefile. I only
> modified r_euterpe_wrap.v target.
>
> Jay
>

From: lisar (Lisa Robinson)

Sent: Friday, December 16, 1994 6:03 PM

To: 'woody (Jay Tomlinson)'

Cc: 'dickson'; 'jeffm'; 'mws'; 'tbr'

Subject: test1 status

Jay Tomlinson wrote (on Fri Dec 16):

testl ran to fab on BOM 194. I used wraprsbim. I modified Makefile and
euterpe_wrap.V so that I could pass RSTPCIBUF through the Makefile. I only
modified r_euterpe_wrap.v target.

Jay

Great,

I pickup up 194 and have test1 running on the zycad too. It
looks to be running ok so far. I also have an ikos version but that is
not so happy.

LIsa R.

From: tbr

Sent: Friday, December 16, 1994 8:40 PM

To: 'lisar (Lisa Robinson)'

Cc: 'billz'

Subject: z redefined

Follow Up Flag: Follow up

Flag Status: Red

Lisa Robinson wrote (on Fri Dec 16):

is this okay


```
gmake[1]: Leaving directory `/N/aphrodite/root/s3/euterpe/verilog/bsrc/au'
gmake[1]: Entering directory `/N/aphrodite/root/s3/euterpe/verilog/bsrc/cc'
cat /n/aphrodite/s3/euterpe/proteus/verilog/diff.h cc.V | /lib/cpp  -P -C -B | sed -e '/^$/d'> cc.v.tmp
376: z redefined
377: z_N redefined
380: z redefined
381: z_N redefined
mv cc.v.tmp cc.v
```

Looks bad to me did you investigate? I cant see anything wrong with
the file that's there now. What version was this?

Tim

From:	tbr
Sent:	Friday, December 16, 1994 9:02 PM
To:	'lisar (Lisa Robinson)'
Cc:	'jeffm'
Subject:	forwarded message from Jeff Marr
Follow Up Flag:	Follow up
Flag Status:	Red

Lisa Robinson wrote (on Fri Dec 16):

------- Start of forwarded message -------
Status: RO
X-VM-v5-Data: ([nil nil nil nil nil nil nil nil nil]
    ["381" "Fri" "16" "December" "1994" "14:29:09" "-0800" "Jeff Marr" "jeffm " nil "8" "SDRAM c model" "^From:"
nil nil "12"])
Return-Path: <jeffm>
Received: from thalia.microunity.com by gaea.microunity.com (4.1/muse1.3)
    id AA05898; Fri, 16 Dec 94 11:07:00 PST
Received: from localhost by thalia.microunity.com (8.6.4/muse-sw.3)
    id OAA11017; Fri, 16 Dec 1994 14:29:09 -0800
Message-Id: <199412162229.OAA11017@thalia.microunity.com>
From: jeffm (Jeff Marr)
To: lisar
Subject: SDRAM c model
Date: Fri, 16 Dec 1994 14:29:09 -0800

What I sent you yesterday is about how it has to be done, per Pat.
I currently can only attach a C model to signals that come out of the
toplevel euterpe_wrap port. Currently this includes only poko,rdata,
and strobe. With the current state of the IKOS tools, I have to bring
the dram interface out thru the wrapper - I cannot instantiate the sdram
c model in the verilog.

In a conversation with Pat, bob and Jay this afternoon they indeed
confirmed that, but siad they will have it fixed in 2.1 in Q195.

I said we can handle it for now, but that in general it will not be
acceptable to not be able to embed a behavioral model inside the gate
level.

Tim

From:	tbr
Sent:	Friday, December 16, 1994 9:09 PM
To:	'woody (Jay Tomlinson)'
Cc:	'dickson'; 'jeffm'; 'lisar'; 'mws'
Subject:	test1 status
Follow Up Flag:	Follow up
Flag Status:	Red

Jay Tomlinson wrote (on Fri Dec 16):

test1 ran to fab on BOM 194. I used wraprsbim. I modified Makefile and
euterpe_wrap.V so that I could pass RSTPCIBUF through the Makefile. I only
modified r_euterpe_wrap.v target.

What's RSTPCIBUF?

Tim

From: Lisa Robinson [lisar@godzilla]

Sent: Friday, December 16, 1994 9:51 PM

To: 'Veena Malwankar'

Cc: 'jeffm@godzilla'; 'tbr@godzilla'

Subject: ikos differences

Veena Malwankar wrote (on Fri Dec 16):

I Looked at IKOS trace that lisar dumped and it seems xlu getting inputs correctly.
I think problem is in xlu_ctrldata and karzes suggested few signal as a fisrt cut.
I am including that list. Please run the test again.

MCsr_amount[6:0]
es/wbus0[127:0]
MCxbus0[63:0]
XLrsltR9[127:0]
xlu/d_6a[127:0]
xlu/G_ctrldata/db_7a[127:0]
xlu/G_ctrldata/dc_8a[127:0]
xlu/G_ctrldata/d_6a[127:0]
xlu/G_ctrldata/dch_6a[127:0]
xlu/G_ctrldata/sdch_6ax[7:0]
uu/vldGoUV
uu/instUV
cr/din_ad0ph
I think above signals are sufficient, if there are more signals it gets too wide.
Thanks

Okay the trace is in
/n/rhodan/s4/euterpe/verilog/bsrc/res/rundpdebug/results/dpemshrspc_0.dpo.2

Lisa R.

From: tbr

Sent: Friday, December 16, 1994 11:06 PM

To: 'hopper (Mark Hofmann)'

Cc: 'tom'; 'solo'; 'wampler'

Subject: Re: VerifyRun snap (fwd)

Follow Up Flag: Follow up

Flag Status: Red

New touble:

done
finished making dependencies -- Fri Dec 16 21:02:43 PST 1994
gmake[1]: Leaving directory `/N/auspex/root/s23/euterpe-proteus-cp/gards'
gmake[1]: Entering directory `/N/auspex/root/s23/euterpe-proteus-cp/gards'
gmake[1]: *** No rule to make target `_MISSING_LAYOUT_FILE_'.
gmake[1]: *** No rule to make target `scxbcgdr1.ly'.
making sofa/ea1porl6nf8s3x4a.pdl -- Fri Dec 16 21:03:07 PST 1994
HOME=/n/auspex/s23/euterpe-proteus-cp/tools CHIPROOT=/n/auspex/s23/euterpe-proteus-cp /n/auspex/s23/euterpe-proteus-cp/tools/bin/piddles -x 'vrr\[.\]' -x vii -r -t mobi234 -c via12 -x vsse -x vdde -x vdda -x vssa -x vcca -g vssc=vssc -g vddc=vddc -g phi_a2p_glob=phi_a2p -g phi_b2p_glob=phi_b2p -g phim_a1p_glob=phim_a1p -g phim_b1p_glob=phim_b1p -g vref_0ph_glob=vref_0ph -v /n/auspex/s23/euterpe-proteus-cp/compass/vlsi.boo-all -V vlsimm_script ea1porl6nf8s3x4a > sofa/ea1porl6nf8s3x4a.pdl.tmp
Translation of /usr/tmp/piddles18677/ea1porl6nf8s3x4a.cif succeeded.
Root symbol is called ROOTCELL.
G

.
.
.

Elapsed wall clock time : 0 Hrs 0 Mins 0 Secs
CHIPROOT=/n/auspex/s23/euterpe-proteus-cp /n/auspex/s23/euterpe-proteus-cp/proteus/gards/basegen/derive_cutouts -v /n/auspex/s23/euterpe-proteus-cp/compass/vlsi.boo-all -c ea1porl8nf8s3x4a -o sofa//ea1porl8nf8s3x4a.cutouts
mv sofa/ea1porl8nf8s3x4a.pdl.tmp sofa/ea1porl8nf8s3x4a.pdl
finished with sofa/ea1porl8nf8s3x4a.pdl -- Fri Dec 16 21:03:54 PST 1994
gmake[1]: Target `sofapdls' not remade because of errors.

Tim

From:	tbr
Sent:	Friday, December 16, 1994 11:41 PM
To:	'hopper (Mark Hofmann)'
Cc:	'solo (John Campbell)'; 'tom (Thomas Laidig)'; 'vant'; 'wampler (Kurt Wampler)'
Subject:	Re: VerifyRun snap (fwd)
Follow Up Flag:	Follow up
Flag Status:	Red

Mark Hofmann wrote (on Fri Dec 16):

Tim B. Robinson writes:
New touble:

done
finished making dependencies -- Fri Dec 16 21:02:43 PST 1994
gmake[1]: Leaving directory `/N/auspex/root/s23/euterpe-proteus-cp/gards'
gmake[1]: Entering directory `/N/auspex/root/s23/euterpe-proteus-cp/gards'
gmake[1]: *** No rule to make target `_MISSING_LAYOUT_FILE_'.
gmake[1]: *** No rule to make target `scxbcgdr1.ly'.
making sofa/ealporl6nf8s3x4a.pdl -- Fri Dec 16 21:03:07 PST 1994
HOME=/n/auspex/s23/euterpe-proteus-cp/tools CHIPROOT=/n/auspex/s23/euterpe-proteus-cp /n/auspex/s23/euterpe-proteus-cp/tools/bin/piddles -x 'vrr\[.\]' -x vii -r -t mobi234 -c via12 -x vsse -x vdde -x vdda -x vssa -x vcca -g vssc=vssc -g vddc=vddc -g phi_a_2p_glob=phi_a2p -g phi_b2p_glob=phi_b2p -g phim_a1p_glob=phim_a1p -g phim_b1p_glob=phim_b1p -g vref_0ph_glob=vref_0ph -v /n/auspex/s23/euterpe-proteus-cp/compass/vlsi.boo-all -V vlsimm_script ealporl6nf8s3x4a > sofa/ealporl6nf8s3x4a.pdl.tmp
Translation of /usr/tmp/piddles18677/ealporl6nf8s3x4a.cif succeeded.
Root symbol is called ROOTCELL.
G
.
.

Elapsed wall clock time : 0 Hrs 0 Mins 0 Secs
CHIPROOT=/n/auspex/s23/euterpe-proteus-cp /n/auspex/s23/euterpe-proteus-cp/proteus/gards/basegen/derive_cutouts -v /n/auspex/s23/euterpe-proteus-cp/compass/vlsi.boo-all -c ealporl8nf8s3x4a -o sofa//ealporl8nf8s3x4a.cutouts
mv sofa/ealporl8nf8s3x4a.pdl.tmp sofa/ealporl8nf8s3x4a.pdl
finished with sofa/ealporl8nf8s3x4a.pdl -- Fri Dec 16 21:03:54 PST 1994
gmake[1]: Target `sofapdls' not remade because of errors.

Hmmm... This seems to be a complaint about scxbcgdr1.ly. That's a new
cell to me. Is there layout that needs to be checked in, does anyone know?

This may not be new after all. I thought the make had died at that
point, but it carried one and is now building gardswarts. So, it's
possible that this problem has been here for a while but has not been
noticed because the make carries on.

Tim

From:	hopper (Mark Hofmann)
Sent:	Saturday, December 17, 1994 12:41 AM
To:	'wampler (Kurt Wampler)'; 'geert (Geert Rosseel)'; 'tbr (Tim B. Robinson)'; 'brianl (Brian Lee)'; 'vo (Tom Vo)'
Subject:	new routing NB results

Hi,

    I didn't save an old log file, so the comparison is somewhat from memory.
However: Last I routed NB it did not converge in 10 iterations. This time it converged in
9 iterations. This 9 iteration result looks very similar in size (i think exactly in
width) to an 9 iteration result i had gotten when i accidentally used an even older
routing strategy (which, however, did worse in other NB situations).

    The initial maze pass seems to consistently pick up 4% of the routes on NB (compared to
7.8% on IFE).

    In conclusion, I would say the NB route is no worse than the best we saw with previous
strategies, but, for NB, is not markedly better.

The make output is available as

       ~hopper/chip/euterpe/verilog/bsrc/nb/out

I think NB may have routed a bit faster. The first dff was written at 21:39, the last iter
dff at 04:28

    -hopper

From: tbr

Sent: Saturday, December 17, 1994 8:44 AM

To: 'hopper (Mark Hofmann)'

Cc: 'brianl (Brian Lee)'; 'geert (Geert Rosseel)'; 'vo (Tom Vo)'; 'Kurt Wampler'

Subject: new routing NB results

Follow Up Flag: Follow up

Flag Status: Red

Mark Hofmann wrote (on Sat Dec 17):

Hi,

I didn't save an old log file, so the comparison is somewhat from memory.
However: Last I routed NB it did not converge in 10 iterations. This time
it converged in 9 iterations. This 9 iteration result looks very similar in
size (i think exactly in width) to an 9 iteration result i had gotten
when i accidentally used an even older routing strategy (which, however,
did worse in other NB situations).

The initial maze pass seems to consistently pick up 4% of the routes on NB
(compared to 7.8% on IFE).

In conclusion, I would say the NB route is no worse than the best we saw
with previous strategies, but, for NB, is not markedly better.

The make output is available as

~hopper/chip/euterpe/verilog/bsrc/nb/out

I think NB may have routed a bit faster. The first dff was written at 21:39,
the last iter dff at 04:28

Sounds like so far we have a net win here. If nothing actually gets
worse (bigger) and things converge more quickly it's definitly worth
it.

Do we have more examples running?

Tim

Mark Hofmann wrote (on Sat Dec 17):

    Hi,

        I didn't save an old log file, so the comparison is somewhat from memory.
    However: Last I routed NB it did not converge in 10 iterations. This time
    it converged in 9 iterations. This 9 iteration result looks very similar in
    size (i think exactly in width) to an 9 iteration result i had gotten
    when i accidentally used an even older routing strategy (which, however,
    did worse in other NB situations).

        The initial maze pass seems to consistently pick up 4% of the routes on NB
    (compared to 7.8% on IFE).

        In conclusion, I would say the NB route is no worse than the best we saw
    with previous strategies, but, for NB, is not markedly better.

    The make output is available as

            ~hopper/chip/euterpe/verilog/bsrc/nb/out

    I think NB may have routed a bit faster. The first dff was written at 21:39,
    the last iter dff at 04:28

Sounds like so far we have a net win here. If nothing actually gets worse (bigger) and
things converge more quickly it's definitly worth it.

Do we have more examples running?

Tim

From: geert (Geert Rosseel)
Sent: Saturday, December 17, 1994 11:00 AM
To: 'vanthof'
Cc: 'hopper'; 'tbr'; 'vo'
Subject: topt problem

Hi Dave,

Topt dies on the top-level euterpe. All the data is in

/n/ghidra/s3/geert/euterpe/verilog/bsrc

The output of the make in in /n/ghidra/s3/geert/euterpe/verilog/bsrc/make.out

I am building geert_euterpe-iter

It looks to me like the strenght file data is not in sync with the
verilog data. I have this before (I think). Can you please look at it.

        Geert

From:	vanthof (vant)
Sent:	Saturday, December 17, 1994 12:21 PM
To:	'Geert Rosseel'
Cc:	'vanthof (Dave Van't Hof)'
Subject:	Re: topt ..

```
Geert Rosseel writes:
>
>
> I moved the gards directory to gards2 and the make.out file to
> make.out2
>
> In my previous run I was pointing to /u/chip/euterpe ... I will start
>up another run pointing to the snapshot euterpe ...
>
>                                  Geert
>
```

Thanks Geert. Sorry about the delay in getting back to you, I slept in this morning.
This looks pretty nasty so it might take a bit to fix.

I'll keep you posted.
Thanks,
Dave

--
Dave Van't Hof   vanthof@microunity.com   MicroUnity Systems Engineering,
Inc.
255 Caspian Way, Sunnyvale, CA (408) 734-8100 X276   #include <std_disclaim.h> Don't blame
me, I didn't vote for him!

.

From: tom (Tom Laidig)

Sent: Saturday, December 17, 1994 3:20 PM

To: 'Tim B. Robinson'

Cc: 'hopper (Mark Hofmann)'; 'solo (John Campbell)'; 'wampler (Kurt Wampler)'; 'Thomas Laidig'

Subject: Re: VerifyRun snap (fwd)

Tim B. Robinson writes:
|
|
|New touble:
|
|done
|### finished making dependencies -- Fri Dec 16 21:02:43 PST 1994
|gmake[1]: Leaving directory `/N/auspex/root/s23/euterpe-proteus-cp/gards'
|gmake[1]: Entering directory `/N/auspex/root/s23/euterpe-proteus-cp/gards'
|gmake[1]: *** No rule to make target `_MISSING_LAYOUT_FILE_'.
|gmake[1]: *** No rule to make target `scxbcgdr1.ly'.

  [snip]

The schematic for scxbcgdr1 seems to have been created on Dec 6 (and
hence it was added to sc-list at that time), but I can find no evidence
that any layout ever existed. Anybody have any idea where this cell
was intended to be used? I'm a little confused by the name, anyway: it
seems that an scxb* cell would be based on some xb* cell, but there's no
xbcgdr1 cell that I've ever heard of. There is a hand-drawn cgdr cell,
but that's the closest I can find.

  --
   ooooO Ooooo
  (_) (_)
   \(tau)/
   ( ) ( )

From:	tbr
Sent:	Saturday, December 17, 1994 6:15 PM
To:	'tom (Tom Laidig)'
Cc:	'hopper (Mark Hofmann)'; 'rich'; 'solo (John Campbell)'; 'tom (Thomas Laidig)'; 'Kurt Wampler'
Subject:	Re: VerifyRun snap (fwd)
Follow Up Flag:	Follow up
Flag Status:	Red

Tom Laidig wrote (on Sat Dec 17):

Tim B. Robinson writes:
|
|
|New touble:
|
|done
|### finished making dependencies -- Fri Dec 16 21:02:43 PST 1994
|gmake[1]: Leaving directory `/N/auspex/root/s23/euterpe-proteus-cp/gards'
|gmake[1]: Entering directory `/N/auspex/root/s23/euterpe-proteus-cp/gards'
|gmake[1]: *** No rule to make target `_MISSING_LAYOUT_FILE_'.
|gmake[1]: *** No rule to make target `scxbcgdr1.ly'.

   [snip]

The schematic for scxbcgdr1 seems to have been created on Dec 6 (and
hence it was added to sc-list at that time), but I can find no evidence
that any layout ever existed. Anybody have any idea where this cell
was intended to be used? I'm a little confused by the name, anyway: it
seems that an scxb* cell would be based on some xb* cell, but there's no
xbcgdr1 cell that I've ever heard of. There is a hand-drawn cgdr cell,
but that's the closest I can find.

Maybe rich knows the history on this one.

Tim

Mark Hofmann wrote ....
>
>
>Hi Kurt,
>
>   I checked in a cahnge to proteus/Makefile.rules and the local
> Makefile
in
>XLU last night and did checked the latter into /u/chip. The output file
is
>given below. It appears that the new routing strategy was not picked up
>for the /u/chip run. I thought that it should be, is there something
>that needs to be updated? [Also I note there is some error in the make
>output regarding a missing VRF file.]
>
>   [For the record, all, ~hopper/chip/euterpe/verilog/bsrc/xlu/out holds
>my local run which shows that XLU did meet timing in 9 iterations with
the
>new routing strategy. Maybe this unintentionally gives a comparison
>point

>for the 2 strategies?] Note that the new routing run completed about
05:10
>this morning, it was started first. The /u/chip run completed at 01:30
and
>was started later.
>
>
>-hopper
>
>ref'ed note:
>--
>--
>Buffalo Chip writes:
>   From chip Sat Dec 17 20:20:43 1994
>   Date: Sun, 18 Dec 1994 01:30:10 -0800
>   From: chip (Buffalo Chip)
>   Message-Id: <199412180930.BAA17250@medusa.microunity.com>
>   To: hopper
>   Subject: output of euterpe/verilog/bsrc/xlu/.checkoutrc
>
>   The output from euterpe/verilog/bsrc/xlu/.checkoutrc is 4016k, so it
is not included
>   in this mail message. Instead, check the file
>
>   /n/tmp/chiplog/hopper.medusa.242.euterpe-verilog-bsrc-xlu
>
>   (which is accessible from all machines). This file will disappear in
>   about 5 days.
>
>   By the way, the exit status returned by .checkoutrc was 0.
>

I looked at your log file . It looks like the rload step was dropped completely .

The /u/chip version (old routing style) completed in 8 iterations while taking slightly
fewer atoms . So we struck out in both time and area improvements with the new strategy .
Could it be because of the dropped rload step .

Mark Hofmann wrote ....
>
>
>Hi Kurt,
>
> I checked in a cahnge to proteus/Makefile.rules and the local
> Makefile
in
>XLU last night and did checked the latter into /u/chip. The output file
is
>given below. It appears that the new routing strategy was not picked up
>for the /u/chip run. I thought that it should be, is there something
>that needs to be updated? [Also I note there is some error in the make
>output regarding a missing VRF file.]

The euterpe gards and clockbias stuffs need to be updated I think .

tvo

From:	tbr
Sent:	Monday, December 19, 1994 11:52 AM
To:	'tom (Tom Laidig)'
Cc:	'brianl (Brian Lee)'
Subject:	lpe mail
Follow Up Flag:	Follow up
Flag Status:	Red

I finally got to look at this one. Is it now a stale issue?

Tim

Tom Laidig wrote (on Mon Dec 5):

> Chip received the attached mail as a result of running lpe on the leaf
> lobes (this is from the snapshot build that was running over the
> weekend). Unless there was some problem, I assume this mail can be
> flushed.

```
 --
    ooooO   Ooooo
   (  )  (  )
    \(  tau  )/
     ()    ()
```

>From chip Sun Dec 4 13:45:39 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14424; Sun, 4 Dec 1994 13:45:39 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16164; Sun, 4 Dec 1994 13:45:35 -0800
Date: Sun, 4 Dec 1994 13:45:35 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042145.NAA16164@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: OR

----------------------- Start of Message -----------------------
>From root Sun Dec 4 13:45:35 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16160; Sun, 4 Dec 1994 13:45:34 -0800
Date: Sun, 4 Dec 1994 13:45:34 -0800
From: root (Charlie Root)
Message-Id: <199412042145.NAA16160@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: buf1x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: buf1x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                  *
*       IIIIII  SSSSSS  SSSSSS            *
*         I    S    S              *
*         I    S    S              *
*         I     SSSSS   SSSSS             *
*         I        S   S          *
*         I        S   S          *
*       IIIIIII SSSSSS  SSSSSS             *
*                                  *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:45:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c buf1x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 16061.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& buf1x1.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2   7/21/94
        lsh: 2.4.15   8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17   7/11/94
VeriCheck is done.

VeriCheck (R) Hierarchical Design Verification, BETA 2.4.1
 (C) Copyright 1990, 1991, 1992, 1993, 1994.
 Integrated Silicon Systems, Inc. All rights reserved.
 This product contains confidential information and trade secrets of
 Integrated Silicon Systems, Inc. Any use or disclosure, except as
 authorized in writing by Integrated Silicon Systems, Inc., is
 prohibited. Copyright is claimed in this product as an unpublished
 work, and the copyright notice does not imply publication.

Printing individual version numbers ...

        vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:

TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*        Compare summary        *
grep: BUF1X1.cmpsum: No such file or directory
grep: BUF1X1.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                      **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN BUF1X1.err       **
**                      **
*******************************************
*******************************************
```

cat buf1x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/buf1x1.compare_lpe/buf1x1.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 13:47:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14463; Sun, 4 Dec 1994 13:47:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16277; Sun, 4 Dec 1994 13:47:31 -0800
Date: Sun, 4 Dec 1994 13:47:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042147.NAA16277@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:47:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16273; Sun, 4 Dec 1994 13:47:31 -0800
Date: Sun, 4 Dec 1994 13:47:31 -0800
From: root (Charlie Root)

Message-Id: <199412042147.NAA16273@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: bufl x2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: bufl x2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/******************************************************************/
*                                 *
*        IIIIII  SSSSSS  SSSSSS          *
*          I    S    S                *
*          I    S    S                *
*          I     SSSSS   SSSSS          *
*          I        S    S            *
*          I        S    S            *
*        IIIIII  SSSSSS  SSSSSS          *
*                                 *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:47:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c bufl x2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 16174.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& bufl x2.log
     Running vericheck
          gdsin: 5.1.2 6/22/94
          gdsout: 5.1.8 6/6/94
          herc: 2.4.2 7/21/94
          lsh: 2.4.15 8/18/94
          vc_engine: 2.4.122 8/30/94
          vp: 2.4.17 7/11/94
VeriCheck is done.

Printing individual version numbers ...

vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary          *
grep: BUF1X2.cmpsum: No such file or directory
grep: BUF1X2.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                           **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**        PLEASE LOOK IN BUF1X2.err      **
**                           **
*******************************************
*******************************************
```

cat buf1x2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/buf1x2.compare_lpe/buf1x2.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 13:48:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14471; Sun, 4 Dec 1994 13:48:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16390; Sun, 4 Dec 1994 13:48:33 -0800
Date: Sun, 4 Dec 1994 13:48:33 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042148.NAA16390@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:48:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16386; Sun, 4 Dec 1994 13:48:33 -0800
Date: Sun, 4 Dec 1994 13:48:33 -0800
From: root (Charlie Root)
Message-Id: <199412042148.NAA16386@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: buf1x3
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: buf1x3
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                    *
*      IIIIII  SSSSSS  SSSSSS            *
*         I    S    S                  *
*         I    S    S                  *
*         I    SSSSS   SSSSS              *
*         I       S   S                 *
*         I       S   S                 *
*      IIIIII  SSSSSS  SSSSSS            *
*                                    *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:48:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c buf1x3 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 16287.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& buf1x3.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

VeriCheck (R) Hierarchical Design Verification, BETA 2.4.1
 (C) Copyright 1990, 1991, 1992, 1993, 1994.
 Integrated Silicon Systems, Inc. All rights reserved.

Printing individual version numbers ...

vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary          *
grep: BUF1X3.cmpsum: No such file or directory
grep: BUF1X3.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                             **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN BUF1X3.err      **
**                             **
*******************************************
*******************************************
```

cat buf1x3.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/buf1x3.compare_lpe/buf1x3.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 13:49:38 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id NAA14488; Sun, 4 Dec 1994 13:49:37 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA16503; Sun, 4 Dec 1994 13:49:36 -0800

Date: Sun, 4 Dec 1994 13:49:36 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042149.NAA16503@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:49:36 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16499; Sun, 4 Dec 1994 13:49:36 -0800
Date: Sun, 4 Dec 1994 13:49:36 -0800
From: root (Charlie Root)
Message-Id: <199412042149.NAA16499@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: buf1x4
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: buf1x4
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                    *
*       IIIIII  SSSSSS  SSSSSS              *
*         I   S     S                 *
*         I   S     S                 *
*         I    SSSSS   SSSSS             *
*         I      S   S            *
*         I      S   S                 *
*       IIIIII  SSSSSS  SSSSSS              *
*                                    *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:49:04 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c buf1x4 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 16400.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& buf1x4.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94

vc_engine: 2.4.122 8/30/94
    vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   .   *
grep: BUF1X4.cmpsum: No such file or directory
grep: BUF1X4.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN BUF1X4.err   **
**   **
****
****

cat buf1x4.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/buf1x4.compare_lpe/buf1x4.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 13:50:37 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
      id NAA14509; Sun, 4 Dec 1994 13:50:36 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id NAA16616; Sun, 4 Dec 1994 13:50:34 -0800
Date: Sun, 4 Dec 1994 13:50:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042150.NAA16616@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 13:50:34 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id NAA16612; Sun, 4 Dec 1994 13:50:34 -0800
Date: Sun, 4 Dec 1994 13:50:34 -0800
From: root (Charlie Root)
Message-Id: <199412042150.NAA16612@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: c2e
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: c2e
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/****************************************************************/
*                                     *
*       IIIIII  SSSSSS  SSSSSS              *
*         I    S     S                 *
*         I    S     S                 *
*         I     SSSSS  SSSSS            *
*         I        S     S             *
*         I        S     S             *
*       IIIIII  SSSSSS  SSSSSS              *
*                                     *
/****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:50:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c c2e -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -

A datain.dat -h cell.equiv -I -n 16513.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& c2e.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: C2E.cmpsum: No such file or directory
grep: C2E.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN C2E.err   **
**   **
****

****

cat c2e.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/c2e.compare_lpe/c2e.lpelog

ISS LPE completed

----------------------- End of Message ------------------------

>From chip Sun Dec 4 13:51:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14530; Sun, 4 Dec 1994 13:51:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16731; Sun, 4 Dec 1994 13:51:30 -0800
Date: Sun, 4 Dec 1994 13:51:30 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042151.NAA16731@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message ------------------------
>From root Sun Dec 4 13:51:30 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16727; Sun, 4 Dec 1994 13:51:30 -0800
Date: Sun, 4 Dec 1994 13:51:30 -0800
From: root (Charlie Root)
Message-Id: <199412042151.NAA16727@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: def2x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: def2x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

/***/
*   *
*   IIIIII SSSSSS SSSSSS   *
*   I   S   S   *
*   I   S   S   *
*   I   SSSSS   SSSSS   *
*   I   S S   *
*   I   S S   *
*   IIIIII SSSSSS SSSSSS   *
*   *

```
/****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:51:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c def2x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 16627.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& def2x1.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
```
grep: DEF2X1.cmpsum: No such file or directory
grep: DEF2X1.cmpsum: No such file or directory
```
*******************************************
```

```
*******************************************
*******************************************
**                       **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN DEF2X1.err      **
**                       **
*******************************************
*******************************************
```

cat def2x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/def2x1.compare_lpe/def2x1.lpelog

ISS LPE completed

----------------------- End of Message ------------------------

>From chip Sun Dec 4 13:52:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
      id NAA14551; Sun, 4 Dec 1994 13:52:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id NAA16844; Sun, 4 Dec 1994 13:52:32 -0800
Date: Sun, 4 Dec 1994 13:52:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042152.NAA16844@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message ------------------------
>From root Sun Dec 4 13:52:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id NAA16840; Sun, 4 Dec 1994 13:52:31 -0800
Date: Sun, 4 Dec 1994 13:52:31 -0800
From: root (Charlie Root)
Message-Id: <199412042152.NAA16840@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: ef2x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: ef2x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                    *
*         IIIIII  SSSSSS  SSSSSS            *
```

```
*        I   S      S              *
*        I   S      S              *
*        I   SSSSS  SSSSS              *
*        I     S  S              *
*        I     S  S              *
*        IIIIII SSSSSS  SSSSSS              *
*                          *
/*********************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:52:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c ef2x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 16741.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& ef2x1.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*********************************************
*        Compare summary         *
grep: EF2X1.cmpsum: No such file or directory
grep: EF2X1.cmpsum: No such file or directory
*********************************************


*********************************************
*********************************************
**                          **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN EF2X1.err      **
**                          **
*********************************************
*********************************************
```

cat ef2x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/ef2x1.compare_lpe/ef2x1.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 13:53:35 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14572; Sun, 4 Dec 1994 13:53:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16958; Sun, 4 Dec 1994 13:53:32 -0800
Date: Sun, 4 Dec 1994 13:53:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042153.NAA16958@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 13:53:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA16954; Sun, 4 Dec 1994 13:53:32 -0800
Date: Sun, 4 Dec 1994 13:53:32 -0800
From: root (Charlie Root)
Message-Id: <199412042153.NAA16954@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: ef3x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: ef3x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4

ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                              *
*       IIIIIII  SSSSSS  SSSSSS              *
*          I    S    S              *
*          I    S    S              *
*          I    SSSSS  SSSSS            *
*          I       S    S         *
*          I       S    S         *
*       IIIIIII  SSSSSS  SSSSSS           *
*                              *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:53:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c ef3x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 16855.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& ef3x1.log
     Running vericheck
          gdsin: 5.1.2 6/22/94
          gdsout: 5.1.8 6/6/94
          herc: 2.4.2 7/21/94
          lsh: 2.4.15 8/18/94
          vc_engine: 2.4.122 8/30/94
          vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

     vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
     TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
     TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
     TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
     TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
     TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:

TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
        TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary           *
grep: EF3X1.cmpsum: No such file or directory
grep: EF3X1.cmpsum: No such file or directory
*******************************************
```

```
*******************************************
*******************************************
**                         **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN EF3X1.err     **
**                         **
*******************************************
*******************************************
```

cat ef3x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/ef3x1.compare_lpe/ef3x1.lpelog

ISS LPE completed

----------------------- End of Message -------------------------

>From chip Sun Dec 4 13:54:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14580; Sun, 4 Dec 1994 13:54:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17071; Sun, 4 Dec 1994 13:54:33 -0800
Date: Sun, 4 Dec 1994 13:54:33 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042154.NAA17071@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 13:54:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17067; Sun, 4 Dec 1994 13:54:33 -0800
Date: Sun, 4 Dec 1994 13:54:33 -0800
From: root (Charlie Root)
Message-Id: <199412042154.NAA17067@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: eflatch
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe

Current Layout: eflatch
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/***************************************************************/
*                               *
*       IIIIII  SSSSSS  SSSSSS           *
*         I    S     S              *
*         I    S     S              *
*         I     SSSSS   SSSSS            *
*         I        S    S        *
*         I        S    S        *
*       IIIIII  SSSSSS  SSSSSS           *
*                               *
/***********************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:54:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c eflatch -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 16968.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& eflatch.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: EFLATCH.cmpsum: No such file or directory
grep: EFLATCH.cmpsum: No such file or directory
*******************************************
```

```
*******************************************
*******************************************
**                      **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**        PLEASE LOOK IN EFLATCH.err       **
**                      **
*******************************************
*******************************************
```

cat eflatch.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/eflatch.compare_lpe/eflatch.lpelog

ISS LPE completed

------------------------- End of Message -------------------------

>From chip Sun Dec 4 13:55:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id NAA14597; Sun, 4 Dec 1994 13:55:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA17184; Sun, 4 Dec 1994 13:55:33 -0800
Date: Sun, 4 Dec 1994 13:55:33 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042155.NAA17184@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------- Start of Message -------------------------
>From root Sun Dec 4 13:55:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id NAA17180; Sun, 4 Dec 1994 13:55:33 -0800
Date: Sun, 4 Dec 1994 13:55:33 -0800
From: root (Charlie Root)
Message-Id: <199412042155.NAA17180@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: lat1x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: lat1x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                    *
*        IIIIII  SSSSSS  SSSSSS            *
*          I    S     S                  *
*          I    S     S                  *
*          I      SSSSS    SSSSS             *
*          I          S    S          *
*          I          S    S          *
*        IIIIIII  SSSSSS  SSSSSS           *
*                                    *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:55:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c lat1x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 17081.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& lat1x1.log
     Running vericheck
          gdsin: 5.1.2 6/22/94
          gdsout: 5.1.8 6/6/94
          herc: 2.4.2 7/21/94
          lsh: 2.4.15 8/18/94
          vc_engine: 2.4.122 8/30/94
          vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

     vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
     TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
      TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
      TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
      TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
      TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
      TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
      TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: LAT1X1.cmpsum: No such file or directory
grep: LAT1X1.cmpsum: No such file or directory
*******************************************
```

```
*******************************************
*******************************************
**                         **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**       PLEASE LOOK IN LAT1X1.err      **
**                         **
*******************************************
*******************************************
```

cat lat1x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/lat1x1.compare_lpe/lat1x1.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 13:56:38 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
      id NAA14618; Sun, 4 Dec 1994 13:56:37 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id NAA17297; Sun, 4 Dec 1994 13:56:34 -0800
Date: Sun, 4 Dec 1994 13:56:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042156.NAA17297@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 13:56:34 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id NAA17293; Sun, 4 Dec 1994 13:56:34 -0800

Date: Sun, 4 Dec 1994 13:56:34 -0800
From: root (Charlie Root)
Message-Id: <199412042156.NAA17293@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: lat1x2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: lat1x2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*********************************************************/
*                                *
*      IIIIIII  SSSSSS  SSSSSS           *
*         I    S      S                *
*         I    S      S                *
*         I      SSSSS   SSSSS           *
*         I          S  S            *
*         I          S  S                *
*      IIIIIII  SSSSSS  SSSSSS           *
*                                *
/*********************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:56:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c lat1x2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 17194.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& lat1x2.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

   vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
********************************************
*         Compare summary          *
grep: LAT1X2.cmpsum: No such file or directory
grep: LAT1X2.cmpsum: No such file or directory
********************************************


********************************************
********************************************
**                             **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**        PLEASE LOOK IN LAT1X2.err     **
**                             **
********************************************
********************************************
```

cat lat1x2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/lat1x2.compare_lpe/lat1x2.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 13:57:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
      id NAA14639; Sun, 4 Dec 1994 13:57:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id NAA17410; Sun, 4 Dec 1994 13:57:31 -0800
Date: Sun, 4 Dec 1994 13:57:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042157.NAA17410@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job

Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:57:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17406; Sun, 4 Dec 1994 13:57:30 -0800
Date: Sun, 4 Dec 1994 13:57:30 -0800
From: root (Charlie Root)
Message-Id: <199412042157.NAA17406@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: lat1x3
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: lat1x3
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/********************************************************************/
*                                          *
*      IIIIII  SSSSSS  SSSSSS                  *
*        I   S     S                        *
*        I   S     S                        *
*        I    SSSSS   SSSSS                   *
*        I       S     S                    *
*        I       S     S                    *
*      IIIIII  SSSSSS  SSSSSS                  *
*                                          *
/********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:57:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c lat1x3 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 17307.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& lat1x3.log
        Running vericheck
            gdsin: 5.1.2 6/22/94
            gdsout: 5.1.8 6/6/94
            herc: 2.4.2 7/21/94
            lsh: 2.4.15 8/18/94
            vc_engine: 2.4.122 8/30/94
            vp: 2.4.17 7/11/94
VeriCheck is done.

VeriCheck (R) Hierarchical Design Verification, BETA 2.4.1

Printing individual version numbers ...

  vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
  TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
  TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
  TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
  TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
  TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
  TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
  TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary        *
grep: LAT1X3.cmpsum: No such file or directory
grep: LAT1X3.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                    **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN LAT1X3.err       **
**                    **
*******************************************
*******************************************
```

cat lat1x3.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/lat1x3.compare_lpe/lat1x3.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 13:58:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
  id NAA14660; Sun, 4 Dec 1994 13:58:32 -0800

Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17523; Sun, 4 Dec 1994 13:58:31 -0800
Date: Sun, 4 Dec 1994 13:58:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042158.NAA17523@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 13:58:30 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17519; Sun, 4 Dec 1994 13:58:30 -0800
Date: Sun, 4 Dec 1994 13:58:30 -0800
From: root (Charlie Root)
Message-Id: <199412042158.NAA17519@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: latch
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: latch
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                        *
*       IIIIII  SSSSSS   SSSSSS               *
*         I    S      S                *
*         I    S      S                *
*         I     SSSSS   SSSSS             *
*         I        S      S             *
*         I        S      S             *
*       IIIIII  SSSSSS   SSSSSS              *
*                                        *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:58:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c latch -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 17420.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& latch.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94

herc: 2.4.2   7/21/94
lsh: 2.4.15 8/18/94
vc_engine: 2.4.122 8/30/94
vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*********************************************
*         Compare summary          *
grep: LATCH.cmpsum: No such file or directory
grep: LATCH.cmpsum: No such file or directory
*********************************************


*********************************************
*********************************************
**                    **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN LATCH.err      **
**                    **
*********************************************
*********************************************
```

cat latch.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/latch.compare_lpe/latch.lpelog

ISS LPE completed

Exhibit C9

-------------------- End of Message -----------------------

>From chip Sun Dec 4 13:59:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id NAA14668; Sun, 4 Dec 1994 13:59:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17637; Sun, 4 Dec 1994 13:59:31 -0800
Date: Sun, 4 Dec 1994 13:59:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042159.NAA17637@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

-------------------- Start of Message -----------------------
>From root Sun Dec 4 13:59:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id NAA17633; Sun, 4 Dec 1994 13:59:31 -0800
Date: Sun, 4 Dec 1994 13:59:31 -0800
From: root (Charlie Root)
Message-Id: <199412042159.NAA17633@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: maj
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: maj
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/******************************************************************/
*                                    *
*       IIIIII  SSSSSS  SSSSSS              *
*         I    S     S                 *
*         I    S     S                 *
*         I     SSSSS   SSSSS              *
*         I        S    S          *
*         I        S    S          *
*       IIIIII  SSSSSS  SSSSSS              *
*                                    *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 13:59:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c maj -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 17533.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& maj.log
 Running vericheck
  gdsin: 5.1.2 6/22/94
  gdsout: 5.1.8 6/6/94
  herc: 2.4.2 7/21/94
  lsh: 2.4.15 8/18/94
  vc_engine: 2.4.122 8/30/94
  vp: 2.4.17 7/11/94
VeriCheck is done.

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 Printing individual version numbers ...

  vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
 TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
 TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
 TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
 TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
 TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
 TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
 TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
* Compare summary *
grep: MAJ.cmpsum: No such file or directory
grep: MAJ.cmpsum: No such file or directory
****

****
****
**   **
** THERE ARE OPENS IN YOUR CIRCUIT **
** PLEASE LOOK IN MAJ.err **

```
**                    **
*******************************************
*******************************************
```

cat maj.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/maj.compare_lpe/maj.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:00:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
       id OAA14689; Sun, 4 Dec 1994 14:00:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
       id OAA17750; Sun, 4 Dec 1994 14:00:34 -0800
Date: Sun, 4 Dec 1994 14:00:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042200.OAA17750@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:00:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
       id OAA17746; Sun, 4 Dec 1994 14:00:33 -0800
Date: Sun, 4 Dec 1994 14:00:33 -0800
From: root (Charlie Root)
Message-Id: <199412042200.OAA17746@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: mux2x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: mux2x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/***************************************************************/
*                              *
*       IIIIII  SSSSSS  SSSSSS           *
*         I    S     S                 *
*         I    S     S                 *
*         I     SSSSS   SSSSS            *
*         I        S   S               *
*         I        S   S               *
```

```
 *       IIIIIII  SSSSSS   SSSSSS           *
 *                                       *
 /*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:00:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c mux2x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 17647.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& mux2x1.log

Running vericheck
     gdsin: 5.1.2 6/22/94
     gdsout: 5.1.8 6/6/94
     herc: 2.4.2 7/21/94
     lsh: 2.4.15 8/18/94
     vc_engine: 2.4.122 8/30/94
     vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
 ********************************************
 *         Compare summary        *
 grep: MUX2X1.cmpsum: No such file or directory
 grep: MUX2X1.cmpsum: No such file or directory
 ********************************************
```

```
*******************************************
*******************************************
**                      **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**     PLEASE LOOK IN MUX2X1.err      **
**                      **
*******************************************
*******************************************
```

cat mux2x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/mux2x1.compare_lpe/mux2x1.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:01:37 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
      id OAA14710; Sun, 4 Dec 1994 14:01:36 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id OAA17865; Sun, 4 Dec 1994 14:01:34 -0800
Date: Sun, 4 Dec 1994 14:01:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042201.OAA17865@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:01:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id OAA17861; Sun, 4 Dec 1994 14:01:33 -0800
Date: Sun, 4 Dec 1994 14:01:33 -0800
From: root (Charlie Root)
Message-Id: <199412042201.OAA17861@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: mux2x2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: mux2x2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

/***/

```
*                                       *
*      IIIIII  SSSSSS  SSSSSS              *
*        I    S     S           *
*        I    S     S           *
*        I    SSSSS   SSSSS          *
*        I        S  S      *
*        I        S  S      *
*      IIIIII  SSSSSS  SSSSSS          *
*                                       *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:01:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c mux2x2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 17762.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& mux2x2.log
Running vericheck
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94
    herc: 2.4.2 7/21/94
    lsh: 2.4.15 8/18/94
    vc_engine: 2.4.122 8/30/94
    vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*********************************************
*          Compare summary          *
grep: MUX2X2.cmpsum: No such file or directory
grep: MUX2X2.cmpsum: No such file or directory
*********************************************
```

```
*********************************************
*********************************************
**                              **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN MUX2X2.err       **
**                              **
*********************************************
*********************************************
```

cat mux2x2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/mux2x2.compare_lpe/mux2x2.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:02:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14731; Sun, 4 Dec 1994 14:02:36 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA17978; Sun, 4 Dec 1994 14:02:34 -0800
Date: Sun, 4 Dec 1994 14:02:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042202.OAA17978@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:02:34 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA17974; Sun, 4 Dec 1994 14:02:34 -0800
Date: Sun, 4 Dec 1994 14:02:34 -0800
From: root (Charlie Root)
Message-Id: <199412042202.OAA17974@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: mux3x1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: mux3x1
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss

```
ISSPATH:        /a/iss
ISS_SYSTYPE:   SUN4
ISS_LSERVER:   hestia
```

user: Undefined variable.

```
/********************************************************************/
*                                          *
*       IIIIII  SSSSSS  SSSSSS                    *
*          I    S     S                      *
*          I    S     S                      *
*          I      SSSSS   SSSSS                    *
*          I         S    S                 *
*          I         S    S                 *
*       IIIIII  SSSSSS  SSSSSS                  *
*                                          *
/********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:02:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c mux3x1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 17875.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& mux3x1.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

        vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
        TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
        TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
        TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
        TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary         *
grep: MUX3X1.cmpsum: No such file or directory
grep: MUX3X1.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                      **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**       PLEASE LOOK IN MUX3X1.err     **
**                      **
*******************************************
*******************************************
```

cat mux3x1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/mux3x1.compare_lpe/mux3x1.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:03:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14752; Sun, 4 Dec 1994 14:03:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18091; Sun, 4 Dec 1994 14:03:32 -0800
Date: Sun, 4 Dec 1994 14:03:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042203.OAA18091@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:03:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18087; Sun, 4 Dec 1994 14:03:31 -0800
Date: Sun, 4 Dec 1994 14:03:31 -0800
From: root (Charlie Root)
Message-Id: <199412042203.OAA18087@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: mux3x2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: mux3x2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                    *
*      IIIIIII  SSSSSS   SSSSSS          *
*        I    S      S                *
*        I    S      S                *
*        I      SSSSS    SSSSS            *
*        I        S      S            *
*        I        S      S            *
*      IIIIIII SSSSSS  SSSSSS           *
*                                    *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:03:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c mux3x2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 17988.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& mux3x2.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:

TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*        Compare summary        *
grep: MUX3X2.cmpsum: No such file or directory
grep: MUX3X2.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                    **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN MUX3X2.err       **
**                    **
*******************************************
*******************************************
```

cat mux3x2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/mux3x2.compare_lpe/mux3x2.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:04:35 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14764; Sun, 4 Dec 1994 14:04:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18204; Sun, 4 Dec 1994 14:04:32 -0800
Date: Sun, 4 Dec 1994 14:04:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042204.OAA18204@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:04:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA18200; Sun, 4 Dec 1994 14:04:32 -0800
Date: Sun, 4 Dec 1994 14:04:32 -0800
From: root (Charlie Root)
Message-Id: <199412042204.OAA18200@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or10
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or10
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                               *
*      IIIIII  SSSSSS  SSSSSS           *
*        I    S     S             *
*        I    S     S             *
*        I     SSSSS   SSSSS            *
*        I        S   S           *
*        I        S   S           *
*      IIIIII  SSSSSS  SSSSSS            *
*                               *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:04:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or10 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 18101.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or10.log
        Running vericheck
              gdsin: 5.1.2 6/22/94
              gdsout: 5.1.8 6/6/94
              herc: 2.4.2 7/21/94
              lsh: 2.4.15 8/18/94
              vc_engine: 2.4.122 8/30/94
              vp: 2.4.17 7/11/94
VeriCheck is done.

Printing individual version numbers ...

        vericheck: 2.4.9 8/24/94

. . .

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: OR10.cmpsum: No such file or directory
grep: OR10.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN OR10.err   **
**   **
****
****

cat or10.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or10.compare_lpe/or10.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:05:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14777; Sun, 4 Dec 1994 14:05:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18317; Sun, 4 Dec 1994 14:05:32 -0800
Date: Sun, 4 Dec 1994 14:05:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042205.OAA18317@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:05:32 1994
Return-Path: <root>

Your "at" job "1989" produced the following output:

Working cell: or11
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or11
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                  *
*      IIIIII  SSSSSS  SSSSSS           *
*        I    S     S                 *
*        I    S     S                 *
*        I     SSSSS   SSSSS          *
*        I         S  S             *
*        I         S  S             *
*      IIIIII  SSSSSS  SSSSSS           *
*                                  *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:05:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or11 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 18214.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or11.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

Printing individual version numbers ...

vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
        TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
        TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
        TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
        TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
        TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
        TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*****************************************
*        Compare summary        *
grep: OR11.cmpsum: No such file or directory
grep: OR11.cmpsum: No such file or directory
*****************************************


*****************************************
*****************************************
**                    **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN OR11.err      **
**                    **
*****************************************
*****************************************
```

cat or11.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or11.compare_lpe/or11.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:06:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14798; Sun, 4 Dec 1994 14:06:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18430; Sun, 4 Dec 1994 14:06:32 -0800
Date: Sun, 4 Dec 1994 14:06:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042206.OAA18430@cyclops.microunity.com>

To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:06:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18426; Sun, 4 Dec 1994 14:06:32 -0800
Date: Sun, 4 Dec 1994 14:06:32 -0800
From: root (Charlie Root)
Message-Id: <199412042206.OAA18426@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or12
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or12
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/******************************************************************/
*                                    *
*      IIIIIII  SSSSSS  SSSSSS           *
*        I    S    S    SSSSSS        *
*        I    S    S                *
*        I    SSSSS   SSSSS            *
*        I      S    S          *
*        I      S    S        *
*      IIIIIII  SSSSSS  SSSSSS           *
*                                    *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:06:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or12 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 18327.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or12.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: OR12.cmpsum: No such file or directory
grep: OR12.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN OR12.err   **
**   **
****
****

cat or12.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or12.compare_lpe/or12.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:08:36 1994
Return-Path: <chip>

Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
      id OAA14836; Sun, 4 Dec 1994 14:08:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id OAA18544; Sun, 4 Dec 1994 14:08:34 -0800
Date: Sun, 4 Dec 1994 14:08:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042208.OAA18544@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -------------------------
>From root Sun Dec 4 14:08:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id OAA18540; Sun, 4 Dec 1994 14:08:33 -0800
Date: Sun, 4 Dec 1994 14:08:33 -0800
From: root (Charlie Root)
Message-Id: <199412042208.OAA18540@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or13
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or13
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/******************************************************************/
*                                           *
*       IIIIII  SSSSSS  SSSSSS              *
*         I    S     S                    *
*         I    S     S                    *
*         I     SSSSS   SSSSS               *
*         I       S     S              *
*         I       S     S              *
*       IIIIII  SSSSSS  SSSSSS               *
*                                           *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:08:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or13 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 18441.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or13.log
      Running vericheck

```
    gdsin: 5.1.2 6/22/94
    gdsout: 5.1.8 6/6/94
    herc: 2.4.2  7/21/94
    lsh: 2.4.15  8/18/94
    vc_engine: 2.4.122  8/30/94
    vp: 2.4.17  7/11/94
VeriCheck is done.
```

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary         *
grep: OR13.cmpsum: No such file or directory
grep: OR13.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                      **
**    THERE ARE OPENS IN YOUR CIRCUIT   **
**       PLEASE LOOK IN OR13.err      **
**                      **
*******************************************
*******************************************
```

cat or13.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or13.compare_lpe/or13.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:09:35 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14857; Sun, 4 Dec 1994 14:09:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18658; Sun, 4 Dec 1994 14:09:33 -0800
Date: Sun, 4 Dec 1994 14:09:33 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042209.OAA18658@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:09:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18654; Sun, 4 Dec 1994 14:09:32 -0800
Date: Sun, 4 Dec 1994 14:09:32 -0800
From: root (Charlie Root)
Message-Id: <199412042209.OAA18654@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or14
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or14
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                        *
*       IIIIIII  SSSSSS  SSSSSS                  *
*          I    S      S                 *
*          I    S      S                 *
*          I     SSSSS    SSSSS                  *
*          I        S      S             *
*          I        S      S             *
*       IIIIIII  SSSSSS  SSSSSS                  *
*                                        *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:09:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or14 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -l -n 18555.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or14.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: OR14.cmpsum: No such file or directory
grep: OR14.cmpsum: No such file or directory
****

****
****
**   **

```
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**      PLEASE LOOK IN OR14.err      **
**                          **
********************************************
********************************************
```

cat or14.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or14.compare_lpe/or14.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:10:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14865; Sun, 4 Dec 1994 14:10:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18771; Sun, 4 Dec 1994 14:10:32 -0800
Date: Sun, 4 Dec 1994 14:10:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042210.OAA18771@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:10:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18767; Sun, 4 Dec 1994 14:10:31 -0800
Date: Sun, 4 Dec 1994 14:10:31 -0800
From: root (Charlie Root)
Message-Id: <199412042210.OAA18767@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or15
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or15
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                  *
*      IIIIII  SSSSSS  SSSSSS            *
*         I   S    S               *
*         I   S    S               *
*         I    SSSSS  SSSSS          *
```

```
*       I    S    S          *
*       I    S    S          *
*      IIIIII SSSSSS SSSSSS          *
*                            *
/*************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:10:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or15 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null
-A datain.dat -h cell.equiv -I -n 18668.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or15.log
　　　Running vericheck
　　　　　　gdsin: 5.1.2 6/22/94
　　　　　　gdsout: 5.1.8 6/6/94
　　　　　　herc: 2.4.2 7/21/94
　　　　　　lsh: 2.4.15 8/18/94
　　　　　　vc_engine: 2.4.122 8/30/94
　　　　　　vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

　　　vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
　　　TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
　　　TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
　　　TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
　　　TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
　　　TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
　　　TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
　　　TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
******************************************
*        Compare summary        *
```
grep: OR15.cmpsum: No such file or directory

grep: OR15.cmpsum: No such file or directory
****


```
*********************************************
*********************************************
**                      **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**      PLEASE LOOK IN OR15.err      **
**                      **
*********************************************
*********************************************
```

cat or15.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or15.compare_lpe/or15.lpelog

ISS LPE completed

----------------------- End of Message ------------------------

>From chip Sun Dec 4 14:11:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14882; Sun, 4 Dec 1994 14:11:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18885; Sun, 4 Dec 1994 14:11:31 -0800
Date: Sun, 4 Dec 1994 14:11:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042211.OAA18885@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message ------------------------
>From root Sun Dec 4 14:11:30 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18881; Sun, 4 Dec 1994 14:11:30 -0800
Date: Sun, 4 Dec 1994 14:11:30 -0800
From: root (Charlie Root)
Message-Id: <199412042211.OAA18881@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or16
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or16
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/******************************************************************/
*                                    *
*      IIIIIII  SSSSSS  SSSSSS              *
*        I    S     S                *
*        I    S     S                *
*        I    SSSSS  SSSSS              *
*        I       S    S              *
*        I       S    S              *
*      IIIIIII  SSSSSS  SSSSSS              *
*                                    *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:11:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or16 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 18782.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& or16.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

        vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
        TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
        TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
        TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
        TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
        TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:

TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*         Compare summary         *
grep: OR16.cmpsum: No such file or directory
grep: OR16.cmpsum: No such file or directory
*******************************************
```

```
*******************************************
*******************************************
**                          **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**       PLEASE LOOK IN OR16.err      **
**                          **
*******************************************
*******************************************
```

cat or16.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or16.compare_lpe/or16.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:12:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14903; Sun, 4 Dec 1994 14:12:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18998; Sun, 4 Dec 1994 14:12:30 -0800
Date: Sun, 4 Dec 1994 14:12:30 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042212.OAA18998@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:12:30 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA18994; Sun, 4 Dec 1994 14:12:30 -0800
Date: Sun, 4 Dec 1994 14:12:30 -0800
From: root (Charlie Root)
Message-Id: <199412042212.OAA18994@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or17
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or17
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

```
LTLPATH:        /a/iss
ISSPATH:        /a/iss
ISS_SYSTYPE:   SUN4
ISS_LSERVER:   hestia
```

user: Undefined variable.

```
/*********************************************************************/
*                                      *
*       IIIIII  SSSSSS  SSSSSS              *
*         I    S    S                  *
*         I    S    S                  *
*         I     SSSSS   SSSSS               *
*         I       S   S             *
*         I       S   S             *
*       IIIIIII  SSSSSS  SSSSSS              *
*                                      *
/*********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:12:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or17 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 18895.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& or17.log

Running vericheck
     gdsin: 5.1.2 6/22/94
     gdsout: 5.1.8 6/6/94
     herc: 2.4.2 7/21/94
     lsh: 2.4.15 8/18/94
     vc_engine: 2.4.122 8/30/94
     vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

     vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
     TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
     TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
     TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
     TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*        Compare summary        *
grep: OR17.cmpsum: No such file or directory
grep: OR17.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                      **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN OR17.err       **
**                      **
*******************************************
*******************************************
```

cat or17.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or17.compare_lpe/or17.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:13:33 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA14924; Sun, 4 Dec 1994 14:13:32 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19111; Sun, 4 Dec 1994 14:13:31 -0800
Date: Sun, 4 Dec 1994 14:13:31 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042213.OAA19111@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:13:31 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19107; Sun, 4 Dec 1994 14:13:31 -0800
Date: Sun, 4 Dec 1994 14:13:31 -0800
From: root (Charlie Root)
Message-Id: <199412042213.OAA19107@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or2

Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                    *
*       IIIIIII   SSSSSS   SSSSSS           *
*          I      S     S                   *
*          I      S     S                   *
*          I      SSSSS   SSSSS           *
*          I          S  S          *
*          I          S  S          *
*       IIIIIII   SSSSSS   SSSSSS          *
*                                    *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:13:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 19008.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or2.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2   7/21/94
        lsh: 2.4.15   8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

        vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*********************************************
*          Compare summary          *
grep: OR2.cmpsum: No such file or directory
grep: OR2.cmpsum: No such file or directory
*********************************************


*********************************************
*********************************************
**                          **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**        PLEASE LOOK IN OR2.err        **
**                          **
*********************************************
*********************************************
```

cat or2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or2.compare_lpe/or2.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:14:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14945; Sun, 4 Dec 1994 14:14:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA19224; Sun, 4 Dec 1994 14:14:32 -0800
Date: Sun, 4 Dec 1994 14:14:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042214.OAA19224@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:14:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA19220; Sun, 4 Dec 1994 14:14:31 -0800
Date: Sun, 4 Dec 1994 14:14:31 -0800
From: root (Charlie Root)
Message-Id: <199412042214.OAA19220@cyclops.microunity.com>

To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or3
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or3
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                    *
*         IIIIIII  SSSSSS   SSSSSS            *
*            I    S     S    S     S          *
*            I    S     S    S                *
*            I    SSSSS    SSSSS              *
*            I        S    S            S     *
*            I        S    S            S     *
*            IIIIIII  SSSSSS   SSSSSS         *
*                                    *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:14:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or3 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 19121.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or3.log
      Running vericheck
            gdsin: 5.1.2 6/22/94
            gdsout: 5.1.8 6/6/94
            herc: 2.4.2 7/21/94
            lsh: 2.4.15 8/18/94
            vc_engine: 2.4.122 8/30/94
            vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
   TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
   TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
   TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
   TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
   TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
   TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
   TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****
*   Compare summary   *
grep: OR3.cmpsum: No such file or directory
grep: OR3.cmpsum: No such file or directory
****

****
****
**   **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**   PLEASE LOOK IN OR3.err   **
**   **
****
****

cat or3.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or3.compare_lpe/or3.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:15:35 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
      id OAA14961; Sun, 4 Dec 1994 14:15:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id OAA19338; Sun, 4 Dec 1994 14:15:32 -0800
Date: Sun, 4 Dec 1994 14:15:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042215.OAA19338@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------

Your "at" job "1989" produced the following output:

Working cell: or4
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or4
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*****************************************************************/
*                                       *
*     IIIIIII  SSSSSS  SSSSSS               *
*        I   S    S                  *
*        I   S    S                  *
*        I    SSSSS   SSSSS                *
*        I       S   S               *
*        I       S   S               *
*     IIIIIII  SSSSSS  SSSSSS               *
*                                       *
/*****************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:15:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or4 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 19234.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or4.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: OR4.cmpsum: No such file or directory
grep: OR4.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                         **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN OR4.err        **
**                         **
*******************************************
*******************************************
```

cat or4.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or4.compare_lpe/or4.lpelog

ISS LPE completed

------------------------- End of Message -------------------------

>From chip Sun Dec 4 14:16:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14974; Sun, 4 Dec 1994 14:16:36 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA19451; Sun, 4 Dec 1994 14:16:34 -0800
Date: Sun, 4 Dec 1994 14:16:34 -0800

From: chip (Buffalo Chip)
Message-Id: <199412042216.OAA19451@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:16:34 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19447; Sun, 4 Dec 1994 14:16:34 -0800
Date: Sun, 4 Dec 1994 14:16:34 -0800
From: root (Charlie Root)
Message-Id: <199412042216.OAA19447@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or5
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or5
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/********************************************************************/
*                                    *
*       IIIIIII  SSSSSS   SSSSSS              *
*         I    S      S               *
*         I    S      S               *
*         I     SSSSS    SSSSS              *
*         I        S      S               *
*         I        S      S               *
*       IIIIIII  SSSSSS   SSSSSS              *
*                                    *
/********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:16:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or5 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 19348.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or5.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94

vp: 2.4.17   7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: OR5.cmpsum: No such file or directory
grep: OR5.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                        **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**      PLEASE LOOK IN OR5.err      **
**                        **
*******************************************
*******************************************
```

cat or5.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or5.compare_lpe/or5.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:17:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
    id OAA14995; Sun, 4 Dec 1994 14:17:34 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA19565; Sun, 4 Dec 1994 14:17:32 -0800
Date: Sun, 4 Dec 1994 14:17:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042217.OAA19565@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:17:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
    id OAA19561; Sun, 4 Dec 1994 14:17:32 -0800
Date: Sun, 4 Dec 1994 14:17:32 -0800
From: root (Charlie Root)
Message-Id: <199412042217.OAA19561@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or6
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or6
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/*******************************************************************/
*                                    *
*      IIIIIII  SSSSSS  SSSSSS          *
*         I    S      S                 *
*         I    S      S                 *
*         I     SSSSS   SSSSS             *
*         I        S      S             *
*         I        S      S             *
*      IIIIIII  SSSSSS  SSSSSS          *
*                                    *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:17:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or6 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 19462.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-

cp/tools/lib/stream/mobimos1.tbl >>& or6.log
   Running vericheck
         gdsin: 5.1.2 6/22/94
         gdsout: 5.1.8 6/6/94
         herc: 2.4.2 7/21/94
         lsh: 2.4.15 8/18/94
         vc_engine: 2.4.122 8/30/94
         vp: 2.4.17 7/11/94
   VeriCheck is done.

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   Printing individual version numbers ...

         vericheck: 2.4.9 8/24/94

   VERICHECK WARNING : At or near line 399:
         TEMP layer "notmet23ped" defined but never used

   VERICHECK WARNING : At or near line 398:
         TEMP layer "notmet34ped" defined but never used

   VERICHECK WARNING : At or near line 412:
         TEMP layer "n+gateab" defined but never used

   VERICHECK WARNING : At or near line 411:
         TEMP layer "n+gateup" defined but never used

   VERICHECK WARNING : At or near line 400:
         TEMP layer "gatepoly" defined but never used

   VERICHECK WARNING : At or near line 410:
         TEMP layer "p+gateab" defined but never used

   VERICHECK WARNING : At or near line 409:
         TEMP layer "p+gateup" defined but never used

   VeriCheck is done.

   ****
   *   Compare summary   *
   grep: OR6.cmpsum: No such file or directory
   grep: OR6.cmpsum: No such file or directory
   ****

   ****
   ****
   **   **
   **   THERE ARE OPENS IN YOUR CIRCUIT   **
   **   PLEASE LOOK IN OR6.err   **
   **   **
   ****
   ****

cat or6.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or6.compare_lpe/or6.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:18:34 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA15016; Sun, 4 Dec 1994 14:18:33 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19678; Sun, 4 Dec 1994 14:18:32 -0800
Date: Sun, 4 Dec 1994 14:18:32 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042218.OAA19678@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:18:32 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19674; Sun, 4 Dec 1994 14:18:31 -0800
Date: Sun, 4 Dec 1994 14:18:31 -0800
From: root (Charlie Root)
Message-Id: <199412042218.OAA19674@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or7
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or7
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/**************************************************************/
*                                 *
*       IIIIIII  SSSSSS  SSSSSS          *
*          I    S     S                *
*          I    S     S                *
*          I     SSSSS  SSSSS           *
*          I        S     S             *
*          I        S     S             *
*       IIIIIII  SSSSSS  SSSSSS          *
*                                 *
/**************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:18:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or7 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -
A datain.dat -h cell.equiv -I -n 19575.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& or7.log
　　　Running vericheck
　　　　　gdsin: 5.1.2 6/22/94
　　　　　gdsout: 5.1.8 6/6/94
　　　　　herc: 2.4.2 7/21/94
　　　　　lsh: 2.4.15 8/18/94
　　　　　vc_engine: 2.4.122 8/30/94
　　　　　vp: 2.4.17 7/11/94
　　　VeriCheck is done.

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　　　 work, and the copyright notice does not imply publication.

　　　Printing individual version numbers ...

　　　　　vericheck: 2.4.9 8/24/94

　　　VERICHECK WARNING : At or near line 399:
　　　　　TEMP layer "notmet23ped" defined but never used

　　　VERICHECK WARNING : At or near line 398:
　　　　　TEMP layer "notmet34ped" defined but never used

　　　VERICHECK WARNING : At or near line 412:
　　　　　TEMP layer "n+gateab" defined but never used

　　　VERICHECK WARNING : At or near line 411:
　　　　　TEMP layer "n+gateup" defined but never used

　　　VERICHECK WARNING : At or near line 400:
　　　　　TEMP layer "gatepoly" defined but never used

　　　VERICHECK WARNING : At or near line 410:
　　　　　TEMP layer "p+gateab" defined but never used

　　　VERICHECK WARNING : At or near line 409:
　　　　　TEMP layer "p+gateup" defined but never used

　　　VeriCheck is done.

　　　**
　　　*　　　　　Compare summary　　　　　*
　　　grep: OR7.cmpsum: No such file or directory
　　　grep: OR7.cmpsum: No such file or directory
　　　**

　　　**

```
**********************************************
**                        **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN OR7.err      **
**                        **
**********************************************
**********************************************
```

cat or7.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or7.compare_lpe/or7.lpelog

ISS LPE completed

----------------------- End of Message ------------------------

>From chip Sun Dec 4 14:20:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
      id OAA15054; Sun, 4 Dec 1994 14:20:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id OAA19791; Sun, 4 Dec 1994 14:20:34 -0800
Date: Sun, 4 Dec 1994 14:20:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042220.OAA19791@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message ------------------------
>From root Sun Dec 4 14:20:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
      id OAA19787; Sun, 4 Dec 1994 14:20:33 -0800
Date: Sun, 4 Dec 1994 14:20:33 -0800
From: root (Charlie Root)
Message-Id: <199412042220.OAA19787@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or8
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or8
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/***************************************************************/
*                           *
*      IIIIII  SSSSSS  SSSSSS         *
*         I    S     S             *
```

```
*      I   S      S              *
*      I  SSSSS   SSSSS                  *
*      I    S    S              *
*      I    S    S              *
*      IIIIII SSSSSS  SSSSSS            *
*                              *
/*******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:20:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or8 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 19688.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& or8.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
    TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
    TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
    TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
    TEMP layer "p+gateup" defined but never used

VeriCheck is done.

****

```
*       Compare summary        *
grep: OR8.cmpsum: No such file or directory
grep: OR8.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                     **
**   THERE ARE OPENS IN YOUR CIRCUIT    **
**      PLEASE LOOK IN OR8.err       **
**                     **
*******************************************
*******************************************
```

cat or8.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or8.compare_lpe/or8.lpelog

ISS LPE completed

----------------------- End of Message -----------------------

>From chip Sun Dec 4 14:22:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA15075; Sun, 4 Dec 1994 14:22:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19905; Sun, 4 Dec 1994 14:22:34 -0800
Date: Sun, 4 Dec 1994 14:22:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042222.OAA19905@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message -----------------------
>From root Sun Dec 4 14:22:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA19901; Sun, 4 Dec 1994 14:22:33 -0800
Date: Sun, 4 Dec 1994 14:22:33 -0800
From: root (Charlie Root)
Message-Id: <199412042222.OAA19901@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: or9
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: or9
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/******************************************************************/
*                                    *
*       IIIIIII  SSSSSS   SSSSSS            *
*          I    S     S                *
*          I    S     S                *
*          I     SSSSS   SSSSS           *
*          I        S   S            *
*          I        S   S            *
*       IIIIIII  SSSSSS   SSSSSS           *
*                                    *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:22:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c or9 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -o /dev/null -A datain.dat -h cell.equiv -I -n 19802.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl >>& or9.log
Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

        vericheck: 2.4.9   8/24/94

VERICHECK WARNING : At or near line 399:
        TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
        TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
        TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
        TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
        TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
        TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
        TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: OR9.cmpsum: No such file or directory
grep: OR9.cmpsum: No such file or directory
*******************************************
```

```
*******************************************
*******************************************
**                              **
**   THERE ARE OPENS IN YOUR CIRCUIT   **
**      PLEASE LOOK IN OR9.err      **
**                              **
*******************************************
*******************************************
```

cat or9.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/or9.compare_lpe/or9.lpelog

ISS LPE completed

----------------------- End of Message ------------------------

>From chip Sun Dec 4 14:24:40 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
        id OAA15113; Sun, 4 Dec 1994 14:24:39 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA20019; Sun, 4 Dec 1994 14:24:34 -0800
Date: Sun, 4 Dec 1994 14:24:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042224.OAA20019@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

----------------------- Start of Message ------------------------
>From root Sun Dec 4 14:24:34 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
        id OAA20015; Sun, 4 Dec 1994 14:24:34 -0800
Date: Sun, 4 Dec 1994 14:24:34 -0800
From: root (Charlie Root)
Message-Id: <199412042224.OAA20015@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: switch2px1
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: switch2px1

rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/******************************************************************/
*                                    *
*       IIIIII  SSSSSS  SSSSSS             *
*          I    S     S              *
*          I    S     S              *
*          I     SSSSS   SSSSS             *
*          I        S     S          *
*          I        S     S          *
*       IIIIII  SSSSSS  SSSSSS             *
*                                    *
/******************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:24:03 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c switch2px1 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 19916.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& switch2px1.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

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Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
    TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
    TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:

TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
     TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
     TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
     TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*****************************************
*         Compare summary          *
grep: SWITCH2PX1.cmpsum: No such file or directory
grep: SWITCH2PX1.cmpsum: No such file or directory
*****************************************


*****************************************
*****************************************
**                       **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN SWITCH2PX1.err       **
**                       **
*****************************************
*****************************************
```

cat switch2px1.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/switch2px1.compare_lpe/switch2px1.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

>From chip Sun Dec 4 14:25:36 1994
Return-Path: <chip>
Received: from cyclops.microunity.com by clio.microunity.com (8.6.4/muse-sw.3)
     id OAA15134; Sun, 4 Dec 1994 14:25:35 -0800
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id OAA20133; Sun, 4 Dec 1994 14:25:34 -0800
Date: Sun, 4 Dec 1994 14:25:34 -0800
From: chip (Buffalo Chip)
Message-Id: <199412042225.OAA20133@cyclops.microunity.com>
To: tom, doi
Subject: Bounced: Output from "at" job
Status: O

------------------------ Start of Message ------------------------
>From root Sun Dec 4 14:25:33 1994
Return-Path: <root>
Received: from localhost by cyclops.microunity.com (8.6.4/muse-sw.3)
     id OAA20129; Sun, 4 Dec 1994 14:25:33 -0800
Date: Sun, 4 Dec 1994 14:25:33 -0800
From: root (Charlie Root)
Message-Id: <199412042225.OAA20129@cyclops.microunity.com>
To: chip
Subject: Output from "at" job

Your "at" job "1989" produced the following output:

Working cell: switch2px2
Using flow: /n/auspex/s23/euterpe-proteus-cp/technology/mobimos/iss/mobilpe1.met.vc
Translation table for Cif To Stream: /n/auspex/s23/euterpe-proteus-cp/tools/lib/stream/mobimos1.tbl

Current working directory: /usr/local/etc/dracjobs/isslpe
Current Layout: switch2px2
rm: cannot remove `.' or `..'
rm: cannot remove `.' or `..'

LTLPATH: /a/iss
ISSPATH: /a/iss
ISS_SYSTYPE: SUN4
ISS_LSERVER: hestia

user: Undefined variable.

```
/********************************************************************/
*                                    *
*       IIIIIII  SSSSSS  SSSSSS                 *
*          I    S      S                       *
*          I    S      S                       *
*          I      SSSSS   SSSSS                   *
*          I          S      S             *
*          I          S      S             *
*       IIIIIII  SSSSSS  SSSSSS                 *
*                                    *
/********************************************************************/
```

Creating composite LPE explode and flatten lists

Starting date: Sun Dec 4 14:25:02 PST 1994

/n/auspex/s23/euterpe-proteus-cp/tools/bin/cifles -c switch2px2 -v /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/vlsi.boo -
o /dev/null -A datain.dat -h cell.equiv -I -n 20030.txt -e 1 -Y -G BBOX -s 0.05 -x /n/auspex/s23/euterpe-proteus-
cp/tools/lib/stream/mobimos1.tbl >>& switch2px2.log
    Running vericheck
        gdsin: 5.1.2 6/22/94
        gdsout: 5.1.8 6/6/94
        herc: 2.4.2 7/21/94
        lsh: 2.4.15 8/18/94
        vc_engine: 2.4.122 8/30/94
        vp: 2.4.17 7/11/94
VeriCheck is done.

VeriCheck (R) Hierarchical Design Verification, BETA 2.4.1
  (C) Copyright 1990, 1991, 1992, 1993, 1994.
  Integrated Silicon Systems, Inc. All rights reserved.
  This product contains confidential information and trade secrets of
  Integrated Silicon Systems, Inc. Any use or disclosure, except as
  authorized in writing by Integrated Silicon Systems, Inc., is
  prohibited. Copyright is claimed in this product as an unpublished
  work, and the copyright notice does not imply publication.

Printing individual version numbers ...

    vericheck: 2.4.9 8/24/94

VERICHECK WARNING : At or near line 399:
    TEMP layer "notmet23ped" defined but never used

VERICHECK WARNING : At or near line 398:
　　　TEMP layer "notmet34ped" defined but never used

VERICHECK WARNING : At or near line 412:
　　　TEMP layer "n+gateab" defined but never used

VERICHECK WARNING : At or near line 411:
　　　TEMP layer "n+gateup" defined but never used

VERICHECK WARNING : At or near line 400:
　　　TEMP layer "gatepoly" defined but never used

VERICHECK WARNING : At or near line 410:
　　　TEMP layer "p+gateab" defined but never used

VERICHECK WARNING : At or near line 409:
　　　TEMP layer "p+gateup" defined but never used

VeriCheck is done.

```
*******************************************
*          Compare summary          *
grep: SWITCH2PX2.cmpsum: No such file or directory
grep: SWITCH2PX2.cmpsum: No such file or directory
*******************************************


*******************************************
*******************************************
**                            **
**    THERE ARE OPENS IN YOUR CIRCUIT    **
**       PLEASE LOOK IN SWITCH2PX2.err       **
**                            **
*******************************************
*******************************************
```

cat switch2px2.log >> /n/auspex/s23/euterpe-proteus-cp/lpe/lobes/switch2px2.compare_lpe/switch2px2.lpelog

ISS LPE completed

------------------------ End of Message ------------------------

From: woody (Jay Tomlinson)

Sent: Monday, December 19, 1994 12:46 PM

To: 'lisar (Lisa Robinson)'

Cc: 'jeffm'; 'tbr'

Subject: test1

Lisa Robinson wrote (on Sat Dec 17):

I can't get it to run in verilog or on the zycad. It seems to get stuck just
fetching the same octlet from rom over and over again. There is a huge dump on aphrodite /s3/euterpe/verilog/bsrc/test1 *

Lisa R.

Mark, Rich and I iolated a problem in the communication between ife, icc, and cp. I
am running it again locally to try and figure out why I thought it worked the
other day, it shouldn't have worked. Sorry for the inconvience. I will let you
know.
Jay

Hi,

Here are the timing violations of the latest top-level run.

This has everything in it except cp and dr.

More detailed info is in :

/n/ghidra/s3/geert/euterpe/verilog/bsrc/gards/geert_euterpe-top.stat

(look for HARD ERROR)


```
*******
nb to hcl
*******
```

Warning! Cycle time exceeded by 25.15ps using cycle time of 926.00 for Iteration 1   HARD ERROR 1
    Path After Optimization using cycle time of 926.00:
        nb/nbprbarb/Ug2/u0   (xborffb6df32s 32S)   Oport: Q_AND0PF IntDel: 87.80 net: NBhc1prgrant_N   swg: df
delay: 329.22ps (force)   RC delay: 113.35ps   lds: 5 pcap: 38.90ff cap: 511.79ff (ext) m2len: 0.00 m3len: 4299.00
m4len: 0.0
        hc1/u420/Unst_2_3/u0   (xbor8df32s 32S)   Iport: D6_A0PF Oport: Q_AND0PF IntDel: 229.10 net:
hc1/u420/nst_N_2_3   swg: df delay: 27.63ps (force) RC delay: 0.88ps   lds: 3 pcap: 18.81ff cap: 49.61ff (ext) m2len:
0.00 m3len: 168
        hc1/u420/Unst_0/u0   (xborff15df16s 16S)   Iport: D13_A0PF IntDel: 277.40
        Time through Path: 951.15


```
******
nb to uu
******
```

Warning! Cycle time exceeded by 73.58ps using cycle time of 926.00 for Iteration 1   HARD ERROR 2
    Path After Optimization using cycle time of 926.00:

        nb/nbctrl/Udreforreturn/u0   (xborffb3dh24s 24S)   Oport: q_ad0ph IntDel: 89.60 net: nb/dreforreturn_N swg:
dh   delay: 17.85ps (force) RC delay: 0.71ps   lds: 2 pcap: 45.98ff cap: 83.08ff (ext) m2len: 116.00 m3len: 23.00
m4len: 0.00
        nb/bufNBwed/u0 (xbbufdh32s 32S)   Iport: D0_ANDMPH   Oport: q_ad0ph IntDel: 55.50 net: nbWeDX1
swg: dh   delay: 529.23ps (force) RC delay: 362.35ps   lds: 13 pcap: 64.45ff cap: 913.32ff (ext) m2len: 0.00 m3len:
7717.00 m4len: 0.00
        uu/UnbOutBsy/u1 (xbmuxff2df4s 4S)   Iport: SEL_A0PEH<1>   IntDel: 307.40
        Time through Path: 999.58

```
******
cc to ctiod
******
```

Warning! Cycle time exceeded by 300.43ps using cycle time of 926.00 for Iteration 1   HARD ERROR 82
    Path After Optimization using cycle time of 926.00:
        cc/u56/u0   (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 89.50 net: cc/gowtag15   swg: df delay: 51.94ps
(force)   RC delay: 6.22ps   lds: 2 pcap: 20.34ff cap: 118.54ff (ext) m2len: 0.00 m3len: 331.00 m4len: 651.00
        cc/or3_twall/u0 (xbor3dh32s 32S)   Iport: D1_A0PF Oport: q_ad0ph IntDel: 141.70 net: CCtwallR15 swg: dh
delay: 727.08ps (force)   RC delay: 523.79ps   lds: 2 pcap: 13.22ff cap: 1077.47ff (ext) m2len: 0.00 m3len: 9675.00
m4len: 0.00
        ctiod/ff_weall0/u0   (xbffdf4s 4S)   Iport: D0_ADMPH IntDel: 216.20
        Time through Path: 1226.43

```
******
cc to uu
******
```

Warning! Cycle time exceeded by 438.93ps using cycle time of 926.00 for Iteration 1   HARD ERROR 83
    Path After Optimization using cycle time of 926.00:
        cc/u56/u0   (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 89.50 net: cc/gowtag15   swg: df delay: 51.94ps
(force)   RC delay: 6.22ps   lds: 2 pcap: 20.34ff cap: 118.54ff (ext) m2len: 0.00 m3len: 331.00 m4len: 651.00
        cc/or3_twall/u0 (xbor3dh32s 32S)   Iport: D1_A0PF Oport: q_ad0ph IntDel: 141.70 net: CCtwallR15 swg: dh
delay: 727.08ps (force)   RC delay: 523.79ps   lds: 2 pcap: 13.22ff cap: 1077.47ff (ext) m2len: 0.00 m3len: 9675.00
m4len: 0.00
        uu/UvldTdWrtR16/u0   (xbmuxff2dh2s 2S)   Iport: SEL_A0PEH<1>   IntDel: 354.70
        Time through Path: 1364.93

```
******
cc to nb
******
```

Warning! Cycle time exceeded by 65.29ps using cycle time of 926.00 for Iteration 1   HARD ERROR 90
    Path After Optimization using cycle time of 926.00:
        cc/muxff4_16_nbcout/u4 (xbmuxffb4df32s 32S) Oport: Q_AD0PF IntDel: 89.50 net: CCnbcout<4>   swg: df
delay: 460.90ps (force)   RC delay: 188.35ps   lds: 40 pcap: 251.15ff cap: 742.63ff (ext) m2len: 0.00 m3len: 4468.00
m4len: 0.00
        nb/fqueue/nbfqslice0/Un0_5/u0 (xbor3df32s 32S)   Iport: D2_A0PF Oport: Q_AND0PF IntDel: 179.80 net:
nb/fqueue/nbfqslice0/n0_N_5 swg: df delay: 11.79ps (force) RC delay: 0.23ps   lds: 1 pcap: 6.04ff cap: 23.54ff (ext)
m2len: 0.00 m3len: 3.00 m4len: 172.00
        nb/fqueue/nbfqslice0/Un0/u0 (xborff8df16s 16S)   Iport: D5_A0PF IntDel: 249.30
        Time through Path: 991.29

Warning! Cycle time exceeded by 233.56ps using cycle time of 926.00 for Iteration 1   HARD ERROR 112
    Path After Optimization using cycle time of 926.00:
        cc/muxff4_16_nbcout/u4 (xbmuxffb4df32s 32S) Oport: Q_AD0PF IntDel: 89.50 net: CCnbcout<4>   swg: df
delay: 557.64ps (force)   RC delay: 233.49ps   lds: 40 pcap: 395.50ff cap: 886.98ff (ext) m2len: 0.00 m3len: 4468.00
m4len: 0.00
        nb/fqcount/Ucout_0_0/u0 (xbor5df32s 32S)   Iport: D3_A0PF Oport: Q_AND0PF IntDel: 183.90 net:
nb/fqcount/cout_N_0_0 swg: df delay: 50.02ps (force) RC delay: 3.60ps   lds: 2 pcap: 15.49ff cap: 90.19ff (ext) m2len:
0.00 m3len: 266.00 m4len: 481.00
        nb/fqcount/Ucouta_0/u0 (xborff14df12s 12S)   Iport: D0_A0PF IntDel: 278.50
        Time through Path: 1159.56

Warning! Cycle time exceeded by 295.97ps using cycle time of 926.00 for Iteration 1   HARD ERROR 136
    Path After Optimization using cycle time of 926.00:
        cc/muxff4_16_nbcout/u4 (xbmuxffb4df32s 32S) Oport: Q_AD0PF IntDel: 87.80 net: CCnbcout<4>   swg: df
delay: 658.57ps (force)   RC delay: 257.35ps   lds: 40 pcap: 471.77ff cap: 963.25ff (ext) m2len: 0.00 m3len: 4468.00

m4len: 0.00

　　nb/nbctrl/Upushpqhc0m1_2/u0　　(xbor11df32s 32S)　　　Iport: D1_A0PF　Oport: Q_AND0PF　IntDel: 222.30　net:
nb/nbctrl/pushpqhc0m1_N_2　　swg: df delay: 9.49ps (force)　RC delay: 0.07ps　　lds: 1 pcap: 6.06ff　cap: 18.96ff (ext)
m2len: 34.00　m3len: 27.00　m4len: 0.00

　　nb/nbctrl/Upushpqhc0m1/u0　　(xborff8dh6s 6S)　　　　Iport: D2_A0PF　IntDel: 243.80

　　Time through Path: 1221.97

******
gt to at
******

Warning! Cycle time exceeded by 39.44ps using cycle time of 926.00 for Iteration 1　　HARD ERROR 353

　　Path After Optimization using cycle time of 926.00:

　　gt/UsaoutXorR10/u4　　(xbffbdh24s 24S)　　　Oport: q_ad0ph　IntDel: 89.60　net: GIsaOutR10<20>　　swg: dh delay:
201.51ps (force)　　RC delay: 101.74ps　　lds: 5 pcap: 38.99ff　cap: 485.59ff (ext) m2len: 0.00　m3len: 4060.00　m4len:
0.00

　　at/UatPaSel/UpaSel10/u0 (xbmux3df16s 16S)　　　Iport: D2_AND0PH　　Oport: Q_AND0PF　IntDel: 211.10　net:
at/paR10_N<10> swg: df delay: 212.83ps (force) RC delay: 19.54ps　　lds: 2 pcap: 14.81ff　cap: 202.41ff (ext)　m2len:
0.00　m3len: 1481.00　m4len: 395.00

　　at/Upal509EqfefR11/u0　(xborff7df12s 12S)　　　　Iport: D1_A0PF　IntDel: 250.40

　　Time through Path: 965.44

****
at to ctiod
****

Warning! Cycle time exceeded by 324.03ps using cycle time of 926.00 for Iteration 1　　HARD ERROR 379

　　Path After Optimization using cycle time of 926.00:

　　at/UvldStrR15/u0　　(xbffbdh24s 24S)　　　Oport: q_ad0ph　IntDel: 89.60　net: ATvldStrR15　　swg: dh delay:
789.83ps (force)　　RC delay: 561.85ps　　lds: 3 pcap: 23.78ff　cap: 1119.05ff (ext) m2len: 0.00　m3len: 9957.00　m4len:
0.0

　　ctiod/dor2_d0/u0　　(xbmux2dh16s 16S)　　Iport: SEL_A0PEH<1>　Oport: q_ad0ph　IntDel: 111.40　net:
ctiod/d0　　swg: dh delay: 5.20ps (force) RC delay: 0.02ps　　lds: 1 pcap: 7.80ff　cap: 13.50ff (ext) m2len: 19.00
m3len: 0.00　m4len: 0.00

　　ctiod/muxff2_32dinlo/u0 (xbmuxff2df4s forced 4S)　　　　Iport: D1_AD0PH IntDel: 254.00

　　Time through Path: 1250.03

****
at to uu
****

Warning! Cycle time exceeded by 275.64ps using cycle time of 926.00 for Iteration 1　　HARD ERROR 386

　　Path After Optimization using cycle time of 926.00:

　　at/UvldStrR15/u0　　(xbffbdh24s 24S)　　　Oport: q_and0ph　IntDel: 89.20　net: ATvldStrR15_N　　swg: dh delay:
818.44ps (force)　　RC delay: 562.87ps　　lds: 3 pcap: 23.16ff　cap: 1119.86ff (ext) m2len: 0.00　m3len: 9970.00　m4len:
0.00

　　uu/UvldTdWrtR16/u0　　(xbmuxff2dh2s 2S)　　　Iport: D0_AND0PH　　IntDel: 294.00

　　Time through Path: 1201.64

****
at to cc
****

Warning! Cycle time exceeded by 180.59ps using cycle time of 926.00 for Iteration 1　　HARD ERROR 389

　　Path After Optimization using cycle time of 926.00:

　　at/Uatpadcd/Uillgl/u0　(xborffb14dh24s 24S)　Oport: q_and0ph　IntDel: 200.00　net: LTilglAdrR12　　swg: dh delay:
421.32ps (force)　　RC delay: 245.91ps　　lds: 7 pcap: 51.16ff　cap: 751.75ff (ext) m2len: 0.00　m3len: 6369.00　m4len:

0.00

cc/ccstart/Uforcebad_0/u0   (xbor6df32s 32S)   Iport: D2_A0PF Oport: Q_AND0PF IntDel: 172.70 net:
cc/ccstart/forcebad_N_0   swg: df delay: 32.26ps (force) RC delay: 1.38ps   lds: 7 pcap: 38.17ff cap: 70.37ff (ext)
m2len: 0.00 m3len: 34.00 m4len: 288.00
cc/ccstart/UaSelc4/u0 (xborff5dh8s 8S)   Iport: D2_A0PF IntDel: 280.30
Time through Path: 1106.59

Warning! Cycle time exceeded by 16.64ps using cycle time of 926.00 for Iteration 1   HARD ERROR 408
Path After Optimization using cycle time of 926.00:
at/Uatpadcd/Uillgl/u0 (xborffb14dh24s 24S)   Oport: q_and0ph IntDel: 200.00 net: LTilglAdrR12   swg: dh delay:
430.84ps (force)   RC delay: 252.16ps   lds: 7 pcap: 65.17ff cap: 765.76ff (ext) m2len: 0.00 m3len: 6369.00 m4len:
0.00
cc/ccstart/Uimissout/u0 (xborff4df32s 32S)   Iport: D2_A0PF IntDel: 311.80
Time through Path: 942.64

****
es to mst
****

Warning! Cycle time exceeded by 7.64ps using cycle time of 926.00 for Iteration 1   HARD ERROR 409
Path After Optimization using cycle time of 926.00:
es/u13/u0   (xbffbdh24s 24S)   Oport: q_ad0ph IntDel: 89.20 net: EShotcarry swg: dh delay: 579.04ps (force)
RC delay: 372.32ps   lds: 1 pcap: 8.94ff   cap: 907.75ff (ext) m2len: 0.00 m3len: 8171.00 m4len: 0.00
mst/u00/u27/u0 (xbmuxff2dh12s 12S)   Iport: D0_AD0PH IntDel: 265.40
Time through Path: 933.64

****
au to ctiod
****

Warning! Cycle time exceeded by 23.20ps using cycle time of 926.00 for Iteration 1   HARD ERROR 411
Path After Optimization using cycle time of 926.00:
au/u112/u0   (xbmuxffb2dh24s 24S) Oport: q_ad0ph IntDel: 89.20 net: AUndx1500R2<6>   swg: dh delay:
606.00ps (force)   RC delay: 391.81ps   lds: 5 pcap: 37.98ff cap: 940.20ff (ext) m2len: 0.00 m3len: 8202.00 m4len:
0.00
ctiod/muxff2_8ra/u0   (xbmuxff2df4s 4S)   Iport: D1_AD0PH IntDel: 254.00
Time through Path: 949.20

****
uu to at
****

Warning! Cycle time exceeded by 862.35ps using cycle time of 926.00 for Iteration 1   HARD ERROR 471
Path After Optimization using cycle time of 926.00:
uu/Urst9CUS/u0 (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 89.50 net: UUrstUS swg: df delay: 1258.48ps
(force) RC delay: 767.48ps   lds: 29 pcap: 185.53ff cap: 1361.54ff (ext) m2len: 0.00 m3len: 10691.00 m4len: 0.00
at/UatXcEnblR11/UilglAdrEn_0/u0 (xbor3df32s 32S)   Iport: D2_A0PF Oport: Q_AND0PF IntDel: 165.00 net:
at/UatXcEnblR11/ilglAdrEn_N_0 swg: df delay: 3.27ps (force) RC delay: 0.01ps   lds: 1 pcap: 4.69ff cap: 8.19ff (ext)
m2len: 6.00 m3len: 17.00 m4len: 0.00
at/UatXcEnblR11/UilglAdrEn/u0 (xborff2df4s 4S)   Iport: D0_A0PF IntDel: 272.10
Time through Path: 1788.35

Warning! Cycle time exceeded by 364.29ps using cycle time of 926.00 for Iteration 1   HARD ERROR 1826
Path After Optimization using cycle time of 926.00:

uu/UvldNoXcR11/u0 (xborffb3df32s 32S) Oport: Q_AD0PF IntDel: 87.80 net: UUvldNoXcR11_N swg: df delay: 711.98ps (force) RC delay: 338.59ps lds: 13 pcap: 98.72ff cap: 895.45ff (ext) m2len: 0.00 m3len: 7243.00 m4len: 0.00

at/Uatpadcd/UvldSt_0/u0 (xbor9df32s 32S) Iport: D6_A0PF Oport: Q_AND0PF IntDel: 198.70 net: at/Uatpadcd/vldSt_N_0 swg: df delay: 19.72ps (force) RC delay: 0.41ps lds: 2 pcap: 11.77ff cap: 48.07ff (ext) m2len: 104.00 m3len: 51.00 m4len: 0.00

at/Uatpadcd/UvldSt/u0 (xborff2df2s 2S) Iport: D0_A0PF IntDel: 272.10
Time through Path: 1290.29

****
uu to iq
****

Warning! Cycle time exceeded by 556.43ps using cycle time of 926.00 for Iteration 1 HARD ERROR 470
Path After Optimization using cycle time of 926.00:
uu/Urst9CUS/u0 (xbffbdf32s 32S) Oport: Q_AD0PF IntDel: 90.00 net: UUrstUS swg: df delay: 1215.63ps (force) RC delay: 761.50ps lds: 29 pcap: 177.54ff cap: 1353.55ff (ext) m2len: 0.00 m3len: 10691.00 m4len: 0.00
iq/Urst0C/u0 (xbffbdf8s 8S) Iport: D0_ADMPH IntDel: 176.80
Time through Path: 1482.43

******
uu to lt
******

Warning! Cycle time exceeded by 797.78ps using cycle time of 926.00 for Iteration 1 HARD ERROR 475
Path After Optimization using cycle time of 926.00:
uu/Urst9CUS/u0 (xbffbdf32s 32S) Oport: Q_AD0PF IntDel: 91.30 net: UUrstUS swg: df delay: 1181.17ps (force) RC delay: 775.07ps lds: 29 pcap: 195.68ff cap: 1371.69ff (ext) m2len: 0.00 m3len: 10691.00 m4len: 0.00
lt/UeR0/u0/u0 (xbmuxen2dh16s 16S) Iport: EN_AND0PH Oport: q_and0ph IntDel: 159.10 net: lt/UeR0/u0/m_N swg: dh delay: 4.91ps (force) RC delay: 0.02ps lds: 1 pcap: 7.52ff cap: 12.42ff (ext) m2len: 14.00 m3len: 7.00 m4len: 0.00
lt/UeR0/u0/u1 (xbffdh2s 2S) Iport: D0_ANDMPH IntDel: 287.30
Time through Path: 1723.78

****
uu to gt
****

Warning! Cycle time exceeded by 604.97ps using cycle time of 926.00 for Iteration 1 HARD ERROR 508
Path After Optimization using cycle time of 926.00:
uu/Urst9CUS/u0 (xbffbdf32s 32S) Oport: Q_AD0PF IntDel: 90.00 net: UUrstUS swg: df delay: 1264.17ps (force) RC delay: 795.39ps lds: 29 pcap: 222.83ff cap: 1398.84ff (ext) m2len: 0.00 m3len: 10691.00 m4len: 0.00
gt/Ureset2/u0 (xbffdf8s 8S) Iport: D0_ADMPH IntDel: 176.80
Time through Path: 1530.97

******
uu to cc
******

Warning! Cycle time exceeded by 644.37ps using cycle time of 926.00 for Iteration 1 HARD ERROR 509
Path After Optimization using cycle time of 926.00:
uu/Urst9CUS/u0 (xbffbdf32s 32S) Oport: Q_AD0PF IntDel: 90.00 net: UUrstUS swg: df delay: 1264.17ps (force) RC delay: 795.39ps lds: 29 pcap: 222.83ff cap: 1398.84ff (ext) m2len: 0.00 m3len: 10691.00 m4len: 0.00
cc/ff_rp1/u0 (xbffdf2s 2S) Iport: D0_ADMPH IntDel: 216.20
Time through Path: 1570.37

```
*******
uu to sr
*******
```

Warning! Cycle time exceeded by 816.10ps using cycle time of 926.00 for Iteration 1   HARD ERROR 510
    Path After Optimization using cycle time of 926.00:
        uu/Urst9CUS/u0 (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 91.30 net: UUrstUS   swg: df delay: 1217.67ps
(force) RC delay: 801.63ps   lds: 29 pcap: 231.17ff cap: 1407.18ff (ext) m2len: 0.00 m3len: 10691.00 m4len: 0.00
        sr/u Iport: D1_A0PF Oport: Q_AND0PF IntDel: 158.10 net: sr/u220/mchold_N_1   swg: df delay: 2.94ps (force) RC
delay: 0.00ps   lds: 1 pcap: 4.69ff   cap: 6.79ff (ext) m2len: 7.00 m3len: 0.00 m4len: 0.00
        sr/u220/Umchold/u0   (xborff2df2s 2S)   Iport: D1_A0PF IntDel: 272.10
        Time through Path: 1742.10


```
*******
in uu
******
```

Lot's of timing violations


```
******
uu to rgxmit
******
```

Warning! Cycle time exceeded by 45.81ps using cycle time of 926.00 for Iteration 1   HARD ERROR 1320
    Path After Optimization using cycle time of 926.00:
        uu/holduu/UinSel1CUQ_2/u0   (xborffb4dh24s 24S)   Oport: q_ad0ph IntDel: 89.60 net: uu/inSel1CUQ<2>
swg: dh   delay: 387.51ps (force) RC delay: 234.10ps   lds: 32 pcap: 182.02ff cap: 750.62ff (ext) m2len: 0.00 m3len:
2689.00 m4len: 2997.00
        uu/UinstUQ/u19 (xbmux3dh16s 16S)   Iport: SEL_A0PEH<2>   Oport: q_ad0ph IntDel: 114.00 net:
UUinstUQ<19>   swg: dh delay: 163.00ps (force) RC delay: 45.23ps   lds: 2 pcap: 19.52ff cap: 321.58ff (ext)
m2len: 0.00 m3len: 2746.00 m4len: 0.00
        rgxmit/Ura51RL/u0   (xbffdh24s 24S)   Iport: D0_ADMPH IntDel: 217.70
        Time through Path: 971.81


```
******
uu to mc
******
```

Warning! Cycle time exceeded by 30.01ps using cycle time of 926.00 for Iteration 1   HARD ERROR 1811
    Path After Optimization using cycle time of 926.00:
        uu/UstepUU/u1 (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 90.00 net: UUstepUU<1>   swg: df delay:
649.81ps (force)   RC delay: 348.10ps   lds: 4 pcap: 34.03ff cap: 885.65ff (ext) m2len: 0.00 m3len: 7742.00 m4len:
0.00
        mc/u02/mltstp/u1   (xbffdf4s 4S)   Iport: D0_ADMPH IntDel: 216.20
        Time through Path: 956.01


```
*********
uu to es
*********
```

Warning! Cycle time exceeded by 82.24ps using cycle time of 926.00 for Iteration 1   HARD ERROR 2050
    Path After Optimization using cycle time of 926.00:
        uu/UinstUU/u4 (xbffbdf32s 32S)   Oport: Q_AND0PF IntDel: 90.00 net: UUinstUU_N<4>   swg: df delay:
740.44ps (force)   RC delay: 411.09ps   lds: 6 pcap: 57.06ff cap: 968.96ff (ext) m2len: 0.00 m3len: 8290.00 m4len:
0.00
        es/u02/opcod/u4 (xbffbdf12s 12S)   Iport: D0_ANDMPH   IntDel: 177.80
        Time through Path: 1008.24

From:	geert (Geert Rosseel)
Sent:	Monday, December 19, 1994 5:28 PM
To:	'billz'; 'brianl'; 'dickson'; 'geert'; 'hopper'; 'lisar'; 'mws'; 'tbr'; 'woody'
Subject:	Euterpe top-level status

Hi,

Here is a summary status of the top-level.

I placed the top-level = everything - (cp & dr), ran topt to get the I/O power-level based on the nof file, then reran all the sub-blocks with the new I/O power levels and finally ran the top-level again.

The result looks pretty good and seems like it is going to fit. I also ran the timing analysis and got a bunch of bad paths (I already mailed that out).

The plan for the next run is (with everything in it for the first time) :

1. Move gf, rg and mc about 150 atoms to the right
             Geert

2. Move the XLU to the right until the datapath
      aligns the clock-spar to the right of it.
             Tom

3. Cut 3 rows from the top from sr
      and move sr down with 1 row.
             Brianl

4. Cut 1 row from gt
             Jay

5. Place cc
             Billz

6. Place cp
             Brianl

7. Release dr
             Rich   (this is running now)

Can we do all of this before Tuesday noon ? Then, I can get another top-level done by Wednesday morning.

Also : I think we need to start requiring that a release in a subdirectory always places.
I need to be able to pick up new Euterpe.V releases without being stalled for one or two days until all the placements has been updated. That will be even more necessary as we start wrapping up all the timing errors which will cause lots of small changes at the top-level. I must be able to pick these fixes up as they are released.

                          Geert

From: vo (Tom Vo)
Sent: Monday, December 19, 1994 6:12 PM
To: 'geert (Geert Rosseel)'
Subject: xlu running

```
/n/ghidra/s5/vo/euterpe/verilog/bsrc/xlu .
Look at file log to monitor progress .
```

This version is shifted to the right by 50 atoms

tvo

>From wampler Fri Dec 16 16:58:51 1994
To: agc, billz, brianl, dickson, geert, hopper, mws, ong, tbr, tom, vo,
        wampler, wingard, woody
Subject: New routing strategy unleashed

ATTENTION GARDS USERS:

As part of today's 5:00 "disturbance" we've released a new routing strategy which
significantly changes (and hopefully improves) the routing method.

Routing strategy changes:

  - A new extended-routing-control-file: ".ercf" files are used now in
    place of separate ".rcf" and ".cvp" files. These new .ercf files are
    supported by a new utility of Tom's, "mugroute" -- short for
    MicroUnityGardsROUTE. See the new man page for details.

  - M2Maze pass on shortnets: we now attempt a metal2-only maze route of
    all nets which meet the shortnet criterion of delta-x <= 84 tracks.
    This frees more M3 resource for later long-haul routing.

  - M2 dogleg tolerance increased to 10 tracks during M2/M3 linesearch
    routing: this also frees more M3 resource for later long-haul routing.

  - Linesearch bestescape parameter set to 99: gives the linesearch router
    a better chance of getting around large custom block corner protrusions.

  - M2 comb obstructions during final maze route: delayed-activation
    obstructions are inserted at left/right edges of cells and activated
    during the final 3-layer M2/M3/M4 maze route to prevent the router from
    doing any long-haul routing in M2.

Changed files:

All changes have been released in /u/chip; if you are working out of a local copy or
snapshot, you will need to pick up changes to the following files in order to use the new
strategy:

tools/bin/mugroute
proteus/Makefile.defs
proteus/Makefile.rules
proteus/misc/padtiles.ercf
proteus/misc/spartiles.ercf
proteus/gards/basegen/add_comb
proteus/gards/basegen/sofacdl.c.template
proteus/clockbias/autospar.c.template
proteus/clockbias/clockobs.c
proteus/clockbias/clockobs
euterpe/clockbias/autospar.c
euterpe/clockbias/autospar
euterpe/clockbias/cgclockbias.pdl
euterpe/gards/sofa/sofacdl.c
euterpe/gards/sofa/sofacdl
euterpe/gards/sofa/sofa.cdl
euterpe/gards/verilog/bsrc/Makefile.share

NOTE: some of these files are derived rather than source files; you will need to "gmake"
the appropriate target to get these files updated.

Dear euterpe designers,

More csyn errors have shown up in my latest build of tbr_euterpe-pass1.splvs in
/u/fwo/chip/euterpe/verilog/bsrc. I have used "for" notes to describe similar examples
that are omitted to reduce the length of this file.
See /u/fwo/chip/euterpe/verilog/bsrc/tbr_euterpe-pass1.CSYN for a full listing.
This 20Kbyte file summarizes the 2.2Mbyte csyn error file.

Could those reponsible for the following blocks make the appropriate changes?
Let me know when you have finished the fix so that I can retest euterpe.

Thanks,
Fred.

Absent Verilog Property Check:
  ckf_alp does does not have a swing. Replace with something like ckf_alpfw.

    missing legal node name from cell interface:
       cellname.pin : ioff.ckf_alp
       cellname.pin : ioff.ckf_blp

Floating Input Checks:
ADRS Correctness Check:
  There are 2150 floating internal signals that are neither primary inputs
  or outputs. Even looks like billh has his own signals.

    input
       instance path: top.xiccuioffchipi5u0.vii6
       cellname path: top.xbffdh2s   .vii
    topmost net
       instance path: top.vii6
       cellname path: top.vii6

    Other topmost net cellname paths:
       top.at_cdmisstermr11_0
       top.at_ufrcenblr10_z
       top.at_ufrcenblr10_z_n
       top.at_ugtlbcnflctr8_z
       top.at_ugtlbcnflctr8_z_n
       top.auindx_hi
       top.auindx_lo
       top.billh
       top.billh_n
       top.cc_dor2_8_d0_z   for [0..5]
       top.cc_dor2_8_d0_z_n   for [0..5]
       top.cc_dorff2_vldfillir11_z
       top.cc_dorff2_vldfillir11_z_n
       top.cc_pd
       top.cc_psi13_z
       top.cc_psi13_z_n
       top.cc_pu
       top.cc_u54_z
       top.cc_u54_z_n
       top.cc_u61_z
       top.cc_u61_z_n
       top.cc_z
       top.cc_z_n
       top.cc_za   for [a..e]

```
top.cc_za_n                    for [a..d]
top.cj_sn00_z
top.cj_sn00_z_n
top.cj_sn01_z
top.cj_sn01_z_n
top.cj_we00_z
top.cj_we00_z_n
top.cj_we01_z
top.cj_we01_z_n
top.ck_pd
top.ck_pu
top.cp_ib04_z
top.cp_ib04_z_n
top.cp_ifch21_z
top.cp_ifch21_z_n
top.cp_ifch22_z
top.cp_ifch22_z_n
top.cp_it04_z
top.cp_it04_z_n
top.cp_lstiftch_z
top.cp_lstiftch_z_n
top.cp_pd
top.cp_pu
top.cp_rd02_z
top.cp_rd02_z_n
top.cp_rd04_z
top.cp_rd04_z_n
top.cp_rd06_z
top.cp_rd06_z_n
top.cp_rd08_z
top.cp_rd08_z_n
top.ctiod_dor2_d0_z
top.ctiod_dor2_d0_z_n
top.dr_drbankb0_zero
top.dr_drbankb0_zero_n
top.dr_drbankb1_zero
top.dr_drbankb1_zero_n
top.dr_drout_zeroa        a to i
top.dr_drout_zeroa_n      a to i
...
top.dr_drout_zeroi
top.dr_drout_zeroi_n
top.dr_drreadcount_lastsel_7
top.dr_zeroa
top.dr_zeroa_n
top.dr_zerob
top.dr_zerob_n
top.es_pd
top.es_pu
top.es_u00_u00_u00_z
top.es_u00_u00_u00_z_n
top.es_u00_u00_u01_z
top.es_u00_u00_u01_z_n
...
top.es_u00_u01_u00_z
top.es_u00_u01_u00_z_n
...
top.es_u00_u07_u57_z
top.es_u00_u07_u57_z_n
..
top.es_u01_u00_u00_z
top.es_u01_u00_u00_z_n
...
top.mst_u03_u12_pd
top.mst_u03_u12_pu
top.mst_x06a_z                for 09a,24b,26c,26d,28b,30a..30i
top.mst_x06a_z_n         for 09a,24b,26c,26d,28b,30a..30i
top.nb_dand2_n0_z
```

```
top.nb_dand2_n0_z_n
top.nb_dandff2_drreadyp1_z
top.nb_dandff2_drreadyp1_z_n
top.nb_dandff2_hc0readyp1_z
top.nb_dandff2_hc0readyp1_z_n
top.nb_dandff2_hc1readyp1_z
top.nb_dandff2_hc1readyp1_z_n
top.nb_dandff2_pstore_z
top.nb_dandff2_pstore_z_n
top.nb_dandff2_spreadyp1_z
top.nb_dandff2_spreadyp1_z_n
top.nb_dorff2_dhhisela_z
top.nb_dorff2_dhhisela_z_n
top.nb_dorff2_dhhiselb_z
top.nb_dorff2_dhhiselb_z_n
top.nb_pqueuedrhp_pqptr_zero_n
top.nb_pqueuedrhp_zero
top.nb_pqueuedrlp_pqptr_zero_n
top.nb_pqueuedrlp_zero
top.nb_pqueuehc0_pqptr_zero_n
top.nb_pqueuehc0_zero
top.nb_pqueuehc1_pqptr_zero_n
top.nb_pqueuehc1_zero
top.nb_pqueuesp_pqptr_zero_n
top.nb_pqueuesp_zero
top.nb_rqueue_rqptr_zero_n
top.nb_rqueue_zero
top.nb_za
top.nb_za_n
...
top.nb_zh
top.nb_zh_n
top.nb_zero
top.nb_zero_n
top.pads_low1
top.pads_low1_n
top.pads_low2
top.pads_low2_n
top.pads_low3
top.pads_low3_n
top.rg_rgcr_udstwenblnoprblmwm_z
top.rg_rgcr_udstwenblnoprblmwm_z_n
top.rg_rgcr_uprblmwl_z
top.rg_rgcr_uprblmwl_z_n
top.rg_rgcr_z0c
top.rg_rgcr_z0c_n
top.rg_rgimm_ubrimmbckrr_z
top.rg_rgimm_ubrimmbckrr_z_n
top.rg_rgimm_z0c
top.rg_rgimm_z0c_n
top.rg_rgpc_z0c
top.rg_rgpc_z0c_n
...
top.rg_rgpc_z17c
top.rg_rgpc_z17c_n
top.rgxmit_uctdprblmwl_z
top.rgxmit_uctdprblmwl_z_n
top.rgxmit_umisifpivabckb7_z
top.rgxmit_umisifpivabckb7_z_n
top.rgxmit_uopam2selrq_z
top.rgxmit_uopam2selrq_z_n
top.rgxmit_uopapcenrq_z
top.rgxmit_uopapcenrq_z_n
top.rgxmit_uoparegenrq_z
top.rgxmit_uoparegenrq_z_n
top.rgxmit_uopbimmenrq_z
top.rgxmit_uopbimmenrq_z_n
top.rgxmit_uopbm2selrq_z
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```
top.rgxmit_uopbm2selrq_z_n
top.rgxmit_uopbregenrq_z
top.rgxmit_uopbregenrq_z_n
top.rgxmit_uopbstepzeroorfrcrp_z
top.rgxmit_uopbstepzeroorfrcrp_z_n
top.rgxmit_uopcm2selrq_z
top.rgxmit_uopcm2selrq_z_n
top.rgxmit_uopcregbenrq_z
top.rgxmit_uopcregbenrq_z_n
top.rgxmit_uopcregenrq_z
top.rgxmit_uopcregenrq_z_n
top.rgxmit_uvldundoincr6_z
top.rgxmit_uvldundoincr6_z_n
top.rgxmit_z0c
top.rgxmit_z0c_n
top.sr_z
top.sr_z_n
top.sr_zz02_z
top.sr_zz02_z_n
top.uu_etaokut_0
top.uu_instmicuu_3
top.uu_instmicuu_n_3
top.uu_isrsrvdfgfszuw_n
top.uu_paxcptnunlckr14
top.uu_prblmcdr6_2
top.uu_prblmcdr6_n_2
top.uu_preeminstur_24            for 25,26,27,28,31
top.uu_preeminstur_n_24          for 25,26,27,28,31
top.uu_strr14
top.uu_uimmraw148ut_z
top.uu_uimmraw148ut_z_n
top.uu_uisprblmifenwqu_z
top.uu_uisprblmifenwqu_z_n
top.uu_uisprblmifeut_z
top.uu_uisprblmifeut_z_n
top.uu_unbhiprirjctr14_z
top.uu_unbhiprirjctr14_z_n
top.uu_unbloprirjctr14_z
top.uu_unbloprirjctr14_z_n
top.uu_upaillglxcr13_z
top.uu_upaillglxcr13_z_n
top.uu_urdst00ux_z
top.uu_urdst00ux_z_n
top.uu_uusdrslth10ahduv_z
top.uu_uusdrslth10ahduv_z_n
top.uu_uusdrslth15ahduv_z
top.uu_uusdrslth15ahduv_z_n
top.uu_uusdrslth5ahduv_z
top.uu_uusdrslth5ahduv_z_n
top.uu_uusdrsltl10ahduv_z
top.uu_uusdrsltl10ahduv_z_n
top.uu_uusdrsltl15ahduv_z
top.uu_uusdrsltl15ahduv_z_n
top.uu_uusdrsltl5ahduv_z
top.uu_uusdrsltl5ahduv_z_n
top.uu_uvldnbreqr14_z
top.uu_uvldnbreqr14_z_n
top.uu_uvldnoootrgtexxcr14_z
top.uu_uvldnoootrgtexxcr14_z_n
top.uu_uvldtdwrtr16_z
top.uu_uvldtdwrtr16_z_n
top.uu_uwbckpreemrqstup_z
top.uu_uwbckpreemrqstup_z_n
top.uu_z0c
top.uu_z0c_n
top.vii6
top.vrr6_0
top.vrr6_1
```

```
top.vrr6_2
top.xlu_const_zero_c1_0
top.xlu_const_zero_c1_1
top.xlu_const_zero_c1_n_0
top.xlu_const_zero_c1_n_1
top.xlu_const_zero_c3_0
top.xlu_const_zero_c3_1
top.xlu_const_zero_c3_2
top.xlu_const_zero_c3_3
top.xlu_const_zero_c3_n_0
top.xlu_const_zero_c3_n_1
top.xlu_const_zero_c3_n_2
top.xlu_const_zero_c3_n_3
top.xlu_const_zero_cr_i
top.xlu_const_zero_cr_i_n
top.xlu_const_zero_cr_m
top.xlu_const_zero_cr_m_n
top.xlu_const_zero_cs1_0
top.xlu_const_zero_cs1_1
top.xlu_const_zero_cs1_2
top.xlu_const_zero_cs1_3
top.xlu_const_zero_cs1_n_0
top.xlu_const_zero_cs1_n_1
top.xlu_const_zero_cs1_n_2
top.xlu_const_zero_cs1_n_3
top.xlu_const_zero_cs2_0
top.xlu_const_zero_cs2_n_0
top.xlu_const_zero_cs3_0          for 0..15
top.xlu_const_zero_cs3_n_0        for 0..15
top.xlu_const_zero_zs3_0
top.xlu_const_zero_zs3_1
top.xlu_const_zero_zs3_n_0
top.xlu_const_zero_zs3_n_1
top.xlu_g_sr_control_const_zero
top.xlu_g_sr_control_const_zero_n
top.xlu_g_sr_control_sr_cc1_5a_0
top.xlu_g_sr_control_sr_cc1_5a_n_0
top.xlu_g_sr_masks_const_zero
top.xlu_g_sr_masks_const_zero_n
top.xlu_g_tr_control_xa1_3a_2
top.xlu_g_tr_control_xa1_3a_3
top.xlu_g_tr_control_xa1_3a_7
top.xlu_g_tr_control_xa1_3a_n_2
top.xlu_g_tr_control_xa1_3a_n_3
top.xlu_g_tr_control_xa1_3a_n_7
top.xlu_g_tr_control_xc1_5a_2
top.xlu_g_tr_control_xc1_5a_3
top.xlu_g_tr_control_xc1_5a_7
top.xlu_g_tr_control_xc1_5a_n_2
top.xlu_g_tr_control_xc1_5a_n_3
top.xlu_g_tr_control_xc1_5a_n_7
top.xlu_la_cc1_6a_0
top.xlu_la_cc1_6a_n_0
top.xlu_la_rc1_6a_0
top.xlu_la_rc1_6a_n_0
top.xlu_tr_a1_4a_0
top.xlu_tr_a1_4a_1
top.xlu_tr_a1_4a_2
top.xlu_tr_a1_4a_n_0
top.xlu_tr_a1_4a_n_1
top.xlu_tr_a1_4a_n_2
top.xlu_tr_a2_4a_0
top.xlu_tr_a2_4a_1
top.xlu_tr_a2_4a_2
top.xlu_tr_a2_4a_n_0
top.xlu_tr_a2_4a_n_1
top.xlu_tr_a2_4a_n_2
top.xlu_tr_b1_5a_0
```

```
        top.xlu_tr_b1_5a_1
        top.xlu_tr_b1_5a_2
        top.xlu_tr_b1_5a_3
        top.xlu_tr_b1_5a_n_0
        top.xlu_tr_b1_5a_n_1
        top.xlu_tr_b1_5a_n_2
        top.xlu_tr_b1_5a_n_3
        top.xlu_tr_b2_5a_0
        top.xlu_tr_b2_5a_1
        top.xlu_tr_b2_5a_2
        top.xlu_tr_b2_5a_3
        top.xlu_tr_b2_5a_n_0
        top.xlu_tr_b2_5a_n_1
        top.xlu_tr_b2_5a_n_2
        top.xlu_tr_b2_5a_n_3
        top.xlu_tr_c1_6a_0
        top.xlu_tr_c1_6a_1
        top.xlu_tr_c1_6a_2
        top.xlu_tr_c1_6a_n_0
        top.xlu_tr_c1_6a_n_1
        top.xlu_tr_c1_6a_n_2
        top.xlu_xluadd4_u00_z
        top.xlu_xluadd4_u00_z_n
        top.z0c
        top.z0c_n
        top.zct
        top.zct_n
        top.zsr
        top.zsr_n
----------------------------------------------------------------
Output Shorts Check:
  Net has too many drivers:
    topmost net:
      instance path:      top.mc_u02_maj00x00011
      cellname path:      top.mc_u02_maj00x00011
    drivers:
      instance path:      top.xmcu02mj41u0.mc_u02_maj00x00011
      cellname path:      top.xborff7df4s .q_and0pf
      instance path:      top.xmcu02mj81u0.mc_u02_maj00x00011
      cellname path:      top.xborff7df4s .q_and0pf

    topmost net:
      instance path:      top.mc_u02_min111xx1_n
      cellname path:      top.mc_u02_min111xx1_n
    drivers:
      instance path:      top.xmcu02mn41u0.mc_u02_min111xx1_n
      cellname path:      top.xborff4df8s .q_ad0pf
      instance path:      top.xmcu02mn47u0.mc_u02_min111xx1_n
      cellname path:      top.xborff4df8s .q_ad0pf

    topmost net:
      instance path:      top.mc_u02_min111xx1
      cellname path:      top.mc_u02_min111xx1
    drivers:
      instance path:      top.xmcu02mn41u0.mc_u02_min111xx1
      cellname path:      top.xborff4df8s .q_and0pf
      instance path:      top.xmcu02mn47u0.mc_u02_min111xx1
      cellname path:      top.xborff4df8s .q_and0pf

    topmost net:
      instance path:      top.mc_u02_maj00x00011_n
      cellname path:      top.mc_u02_maj00x00011_n
    drivers:
      instance path:      top.xmcu02mj41u0.mc_u02_maj00x00011_n
      cellname path:      top.xborff7df4s .q_ad0pf
      instance path:      top.xmcu02mj81u0.mc_u02_maj00x00011_n
      cellname path:      top.xborff7df4s .q_ad0pf
----------------------------------------------------------------
```

```
Most Positive Voltage Check:
   Cgeb is still a problem: 1p phi connects to other 2p signals: phi_a2p
      leaf connections:
      ...
         instance path:   top.xclk        .xu103u103.ckrbo_ad1ph
         cellname path:   top.cgclockbias.cgeb       .ckfo_ad1phw
      ...
         instance path:   top.xio0ursou3.phi1west_a2p
         cellname path:   top.scsynchll .phi_a2p
      ...

      Other similar leaf connections that should be 2p:
         instance path:   top.xclk        .xu103u103.ckrbo_bd1ph
         cellname path:   top.cgclockbias.cgeb       .ckfo_bd1phw

         instance path:   top.xclk        .xu102u105.ckrao_ad1ph
         cellname path:   top.cgclockbias.cgeb       .ckfo_ad1phw

         instance path:   top.xclk        .xu102u105.ckrao_bd1ph
         cellname path:   top.cgclockbias.cgeb       .ckfo_bd1phw
--------------------------------------------------------------------
Single Input Swing Check:
   Driver has incompatible swing with input:

      input
         instance path:    top.xgfu05u03ud_6u0.gf_u05_pd
         cellname path:    top.xbor5df2s        .d0_a0pf
      driver: topmost pin
      topmost nets
         instance path:    top.gf_u05_pd
         cellname path:    top.gf_u05_pd

      Other topmost nets, cellname paths:
         cellname path:    top.at_cdmisstermrll_0
         cellname path:    top.cc_ze
         cellname path:    top.gf_u00_pd                  for 00 to 07
         cellname path:    top.gf_u00_pu                  for 00 to 07
         cellname path:    top.gt_ugtsnake_ibwrreq_n_0
         cellname path:    top.gt_ugtsnake_ibwrreq_n_1
         cellname path:    top.hc0z
         cellname path:    top.hc0z_n
         cellname path:    top.hc1z
         cellname path:    top.hc1z_n
         cellname path:    top.nb_pqueuedrhp_pqptr_zero_n
         cellname path:    top.nb_pqueuedrhp_zero
         cellname path:    top.nb_pqueuedrlp_pqptr_zero_n
         cellname path:    top.nb_pqueuedrlp_zero
         cellname path:    top.nb_pqueuehc0_pqptr_zero_n
         cellname path:    top.nb_pqueuehc0_zero
         cellname path:    top.nb_pqueuehc1_pqptr_zero_n
         cellname path:    top.nb_pqueuehc1_zero
         cellname path:    top.nb_pqueuesp_pqptr_zero_n
         cellname path:    top.nb_pqueuesp_zero
         cellname path:    top.nb_rqueue_rqptr_zero_n
         cellname path:    top.nb_rqueue_zero
         cellname path:    top.uu_etaokut_0
         cellname path:    top.uu_isrsrvdfgfszuw_n
         cellname path:    top.uu_paxcptnunlckr14
         cellname path:    top.uu_strr14
         cellname path:    top.uu_z0c
         cellname path:    top.xlu_g_sr_control_sr_cc1_5a_0
         cellname path:    top.xlu_g_tr_control_xa1_3a_2
         cellname path:    top.xlu_g_tr_control_xa1_3a_3
         cellname path:    top.xlu_g_tr_control_xa1_3a_7
         cellname path:    top.xlu_g_tr_control_xc1_5a_2
         cellname path:    top.xlu_g_tr_control_xc1_5a_3
         cellname path:    top.xlu_g_tr_control_xc1_5a_7
--------------------------------------------------------------------
```

```
Exclusive Input Swing Check:
  Drivers fail exclusive input swing requirement:
    Reason: drivers have illegal swing for exclusive in
    exclusive inputs                              for 2u0 to
2u10:
        instance path:     top.xifeucindxi2u0.ife_cindxseli2_3
        cellname path:     top.xbmux4dh2s     .sel_a0peh_3
        instance path:     top.xifeucindxi2u0.ife_cindxseli2_2
        cellname path:     top.xbmux4dh2s     .sel_a0peh_2
        instance path:     top.xifeucindxi2u0.ife_cindxseli2_1
        cellname path:     top.xbmux4dh2s     .sel_a0peh_1
        instance path:     top.xifeucindxi2u0.ife_cindxseli2_0
        cellname path:     top.xbmux4dh2s     .sel_a0peh_0
      drivers
        instance path:     top.xifepcseli1ucindxsel_2u0.ife_cindxseli2_2
        cellname path:     top.xborff2dh8s              .q_ad0ph
        instance path:     top.xifepcseli1ucindxsel_1u0.ife_cindxseli2_1
        cellname path:     top.xborff7dh8s              .q_and0ph
        instance path:     top.xifepcseli1ucindxsel_0u0.ife_cindxseli2_0
        cellname path:     top.xborff5dh8s              .q_ad0ph
      exclusive topmost nets
        instance path:     top.ife_cindxseli2_3
        cellname path:     top.ife_cindxseli2_3
        instance path:     top.ife_cindxseli2_2
        cellname path:     top.ife_cindxseli2_2
        instance path:     top.ife_cindxseli2_1
        cellname path:     top.ife_cindxseli2_1
        instance path:     top.ife_cindxseli2_0
        cellname path:     top.ife_cindxseli2_0


    Reason: drivers have illegal swing for exclusive in
    exclusive inputs
        instance path:
top.xdrdrreadcountmuxff8lastsampleu0.dr_drreadcount_lastsel_7
        cellname path:     top.xbmuxff8df2s                    .sel_a0peh_7
        instance path:
top.xdrdrreadcountmuxff8lastsampleu0.dr_drreadcount_lastsel_6
        cellname path:     top.xbmuxff8df2s                    .sel_a0peh_6
        instance path:
top.xdrdrreadcountmuxff8lastsampleu0.dr_drreadcount_lastsel_5
        cellname path:     top.xbmuxff8df2s                    .sel_a0peh_5
        instance path:
top.xdrdrreadcountmuxff8lastsampleu0.dr_drreadcount_lastsel_4
        cellname path:     top.xbmuxff8df2s                    .sel_a0peh_4
        instance path:
top.xdrdrreadcountmuxff8lastsampleu0.dr_drreadcount_lastsel_3
        cellname path:     top.xbmuxff8df2s                    .sel_a0peh_3
        instance path:
top.xdrdrreadcountmuxff8lastsampleu0.dr_drreadcount_lastsel_2
        cellname path:     top.xbmuxff8df2s                    .sel_a0peh_2
        instance path:
top.xdrdrreadcountmuxff8lastsampleu0.dr_drreadcount_lastsel_1
        cellname path:     top.xbmuxff8df2s                    .sel_a0peh_1
        instance path:
top.xdrdrreadcountmuxff8lastsampleu0.dr_drreadcount_lastsel_0
        cellname path:     top.xbmuxff8df2s                    .sel_a0peh_0
      drivers
        instance path:
top.xdrdrreadcountdrreadcountselulastsel_6u0.dr_drreadcount_lastsel_6
        cellname path:     top.xborff3dh2s
.q_and0ph
        instance path:
top.xdrdrreadcountdrreadcountselulastsel_5u0.dr_drreadcount_lastsel_5
        cellname path:     top.xborff4dh2s
.q_and0ph
        instance path:
top.xdrdrreadcountdrreadcountselulastsel_4u0.dr_drreadcount_lastsel_4
        cellname path:     top.xborff2dh2s
```

```
.q_ad0ph
        instance path:
top.xdrdrreadcountdrreadcountselulastsel_3u0.dr_drreadcount_lastsel_3
        cellname path:      top.xborff2dh2s
.q_ad0ph
        instance path:
top.xdrdrreadcountdrreadcountselulastsel_2u0.dr_drreadcount_lastsel_2
        cellname path:      top.xborff9dh2s
.q_and0ph
        instance path:
top.xdrdrreadcountdrreadcountselulastsel_1u0.dr_drreadcount_lastsel_1
        cellname path:      top.xborff4dh2s
.q_and0ph
        instance path:
top.xdrdrreadcountdrreadcountselulastsel_0u0.dr_drreadcount_lastsel_0
        cellname path:      top.xborff2dh2s
.q_ad0ph
        exclusive topmost nets
        instance path:      top.dr_drreadcount_lastsel_7
        cellname path:      top.dr_drreadcount_lastsel_7
        instance path:      top.dr_drreadcount_lastsel_6
        cellname path:      top.dr_drreadcount_lastsel_6
        instance path:      top.dr_drreadcount_lastsel_5
        cellname path:      top.dr_drreadcount_lastsel_5
        instance path:      top.dr_drreadcount_lastsel_4
        cellname path:      top.dr_drreadcount_lastsel_4
        instance path:      top.dr_drreadcount_lastsel_3
        cellname path:      top.dr_drreadcount_lastsel_3
        instance path:      top.dr_drreadcount_lastsel_2
        cellname path:      top.dr_drreadcount_lastsel_2
        instance path:      top.dr_drreadcount_lastsel_1
        cellname path:      top.dr_drreadcount_lastsel_1
        instance path:      top.dr_drreadcount_lastsel_0
        cellname path:      top.dr_drreadcount_lastsel_0


        Reason: drivers have illegal swing for exclusive in
        exclusive inputs
        instance path:      top.xmcu01u00u200u0.mc_u01_pd0                for u0 to
u7
        cellname path:      top.xbmux2dh2s      .sel_a0peh_1
        instance path:      top.xmcu01u00u200u0.mc_u01_pu0
        cellname path:      top.xbmux2dh2s      .sel_a0peh_0
        drivers
        exclusive topmost nets
        instance path:      top.mc_u01_pd0
        cellname path:      top.mc_u01_pd0
        instance path:      top.mc_u01_pu0
        cellname path:      top.mc_u01_pu0
------------------------------------------------------------------------
Differential Input Swing Check:
        Reason: drivers are non-diff or fail swing check
        diff inputs
        instance path:      top.xsru070u1.aundx1500r2_15
        instance path:      top.xsru070u1.aundx1500r2_15
        cellname path:      top.xbffdf2s .d0_admph
        cellname path:      top.xbffdf2s .d0_andmph
        paired drivers
        instance path:      top.xauindxu20au0.aundx1500r2_15
        instance path:      top.xauindxu20au0.aundx1500r2_15
        cellname path:      top.xbmuxff2df4s .q_ad0pf
        cellname path:      top.xbmuxff2df4s .q_ad0pf
        paired topmost nets
        instance path:      top.aundx1500r2_15
        instance path:      top.aundx1500r2_15
        cellname path:      top.aundx1500r2_15
        cellname path:      top.aundx1500r2_15


        Reason: drivers are non-diff or fail swing check
```

```
     diff inputs
         instance path:      top.xesu02mstpu0.uustepuu_0            For u.*0
to u.*4
         instance path:      top.xesu02mstpu0.uustepuu_0
         cellname path:      top.xbffdf12s     .d0_admph
         cellname path:      top.xbffdf12s     .d0_andmph
     paired drivers
         instance path:      top.xuuustepuuu0.uustepuu_0
         instance path:      top.xuuustepuuu0.uustepuu_0
         cellname path:      top.xbffdf4s      .q_ad0pf
         cellname path:      top.xbffdf4s      .q_ad0pf
     paired topmost nets
         instance path:      top.uustepuu_0
         instance path:      top.uustepuu_0
         cellname path:      top.uustepuu_0
         cellname path:      top.uustepuu_0

     Reason: drivers are non-diff or fail swing check
     diff inputs
         instance path:      top.xrgxmituopbrsltenlrqu1.uustepzeroopbuv_n
         instance path:      top.xrgxmituopbrsltenlrqu1.uustepzeroopbuv_n
         cellname path:      top.xbmuxff2dh2s             .d1_ad0ph
         cellname path:      top.xbmuxff2dh2s             .d1_and0ph
     paired drivers
         instance path:      top.xuuuustepuuuzerobu0.uustepzeroopbuv_n
         instance path:      top.xuuuustepuuuzerobu0.uustepzeroopbuv_n
         cellname path:      top.xborffb4df8s      .q_and0pf
         cellname path:      top.xborffb4df8s      .q_and0pf
     paired topmost nets
         instance path:      top.uustepzeroopbuv_n
         instance path:      top.uustepzeroopbuv_n
         cellname path:      top.uustepzeroopbuv_n
         cellname path:      top.uustepzeroopbuv_n

     Reason: drivers are non-diff or fail swing check
     diff inputs
         instance path:      top.xrgxmituopbrsltenhrqu1.uustepzeroopbuv_n
         instance path:      top.xrgxmituopbrsltenhrqu1.uustepzeroopbuv_n
         cellname path:      top.xbmuxff2dh2s             .d1_ad0ph
         cellname path:      top.xbmuxff2dh2s             .d1_and0ph
     paired drivers
         instance path:      top.xuuuustepuuuzerobu0.uustepzeroopbuv_n
         instance path:      top.xuuuustepuuuzerobu0.uustepzeroopbuv_n
         cellname path:      top.xborffb4df8s      .q_and0pf
         cellname path:      top.xborffb4df8s      .q_and0pf
     paired topmost nets
         instance path:      top.uustepzeroopbuv_n
         instance path:      top.uustepzeroopbuv_n
         cellname path:      top.uustepzeroopbuv_n
         cellname path:      top.uustepzeroopbuv_n
------------------------------------------------------------------------
```

From:	tbr
Sent:	Monday, December 19, 1994 6:59 PM
To:	'fwo (Fred Obermeier)'
Cc:	'fwo'; 'hardheads'
Subject:	More euterpe csyn errors.
Follow Up Flag:	Follow up
Flag Status:	Red

Fred Obermeier wrote (on Mon Dec 19):

Floating Input Checks:
ADRS Correctness Check:
  There are 2150 floating internal signals that are neither primary inputs
  or outputs. Even looks like billh has his own signals.

Has this stuff been through topt? I assume it must have been, but it
looks like a bunch of unused stuff has not been pruned.

Alternatively, are you sure that nothing was in the EXCLUDE list when
you compiled the top level?

Tim

Fred Obermeier wrote (on Mon Dec 19):

    Floating Input Checks:
    ADRS Correctness Check:
      There are 2150 floating internal signals that are neither primary inputs
      or outputs. Even looks like billh has his own signals.

Has this stuff been through topt? I assume it must have been, but it looks like a bunch
of unused stuff has not been pruned.

Alternatively, are you sure that nothing was in the EXCLUDE list when you compiled the top
level?

Tim

Tim,

> Has this stuff been through topt? I assume it must have been, but it
> looks like a bunch of unused stuff has not been pruned.
I remember seeing topt along the way. I don't know what I'm supposed to do to get
pruning. Atleast it didn't happen automatically.

> Alternatively, are you sure that nothing was in the EXCLUDE list when
> you compiled the top level?
The EXCLUDE list is empty: EXCLUDE_LIST_tbr =

My running area can be examined in /u/fwo/chip/euterpe/verilog/bsrc

We still don't know who has done a tribute to BillH by naming a signal after him. And
according to the signal naming convention, that billh_n must be negative BillH. Just what
would a negative billh do?

Thanks,
Fred.

From:	tbr
Sent:	Monday, December 19, 1994 7:13 PM
To:	'fwo'
Cc:	'mws'
Subject:	Re: More euterpe csyn errors.
Follow Up Flag:	Follow up
Flag Status:	Red

Mark Semmelmeyer wrote (on Mon Dec 19):

> I looked at one example of this and the length of the
> list and suspected that all zero one generators are being
> flagged. But I am not sure what is going on because
> non standard net (or cell?) names are being reported
> and I don't know how the procedure works.

The output pin names on 01 generators were changed a while ago to make
them legal. Has this netlist picked up stale versions somehow?

Tim

From:	tbr
Sent:	Monday, December 19, 1994 7:17 PM
To:	'fwo (Fred Obermeier)'
Subject:	Re: More euterpe csyn errors.
Follow Up Flag:	Follow up
Flag Status:	Red

Fred Obermeier wrote (on Mon Dec 19):

Tim,

> Has this stuff been through topt? I assume it must have been, but it
> looks like a bunch of unused stuff has not been pruned.
I remember seeing topt along the way. I don't know what I'm supposed to
do to get pruning. Atleast it didn't happen automatically.

It should do. I think you have to turn on an option to stop it pruning.

> Alternatively, are you sure that nothing was in the EXCLUDE list when
> you compiled the top level?
The EXCLUDE list is empty: EXCLUDE_LIST_tbr =

My running area can be examined in /u/fwo/chip/euterpe/verilog/bsrc

We still don't know who has done a tribute to BillH by naming a signal
after him. And according to the signal naming convention, that billh_n
must be negative BillH. Just what would a negative billh do?

I think you can attribute that one to vo. There is some cell in there
just as a test structure. Dunno about bullh being negative though!

From: fwo (Fred Obermeier)

Sent: Monday, December 19, 1994 7:22 PM

To: 'tbr'

Cc: 'fwo'; 'mws'

Subject: Re: More euterpe csyn errors.

Tim wrote:
Mark Semmelmeyer wrote (on Mon Dec 19):

> I looked at one example of this and the length of the
> list and suspected that all zero one generators are being
> flagged. But I am not sure what is going on because
> non standard net (or cell?) names are being reported
> and I don't know how the procedure works.

> The output pin names on 01 generators were changed a while ago to make
> them legal. Has this netlist picked up stale versions somehow?

All logic cell interface pins have legal names:
```
% grep 'logic[01]' tbr_euterpe-pass1.splvs | fgrep property | sort -u
*@property     pin logic0_ab0pf     output_load (*,*)
*@property     pin logic1_ab0pf     output_load (*,*)
```

There are net names with logic0_0p and logic1_0p in ioclkwart, but that's ok.

Mark, why do think that the floating signals are caused by the 0/1 generators?
Which signal are you looking at?

Thanks,
Fred.

From: fwo (Fred Obermeier)
Sent: Monday, December 19, 1994 7:25 PM
To: 'tbr'
Cc: 'fwo'
Subject: Re: More euterpe csyn errors.

Tim,

> Dunno about bullh being negative though!
I didn't mean that billh was negative.
I just wondered what the negative billh would be used for.

Fred.

From:	tbr
Sent:	Monday, December 19, 1994 7:34 PM
To:	'fwo (Fred Obermeier)'
Cc:	'fwo'
Subject:	Re: More euterpe csyn errors.
Follow Up Flag:	Follow up
Flag Status:	Red

Fred Obermeier wrote (on Mon Dec 19):

Tim,

> Dunno about bullh being negative though!
I didn't mean that billh was negative.
I just wondered what the negative billh would be used for.

You have to talk to vo about that.

Tim

From: fwo (Fred Obermeier)

Sent: Monday, December 19, 1994 7:43 PM

To: 'tbr'

Cc: 'fwo'; 'mws'

Subject: Re: More euterpe csyn errors.

Mark and I poked around a bit more.

We looked for the signal, rgxmit_uctdprblmwl_z.
The ~/chip/proteus/verilog/mlib/dandff2_1.v cell does indeed use a xbc01
generator, but my generated netlist, tbr_euterpe-pass1.splvs, doesn't connect
this cell to a 0/1 generator:

```
xrgxmituctdprblmwlu0    vii6 phi_a2p phi_b2p phi_a2p phi_b2p rgctdprblmwl_n \
  vrr6_2 vrr6_1 vrr6_0 ltcdmissvldr12 ltcdmissvldr12_n
 + rgxmit_uctdprblmwl_z ltcdmiss2cr12 rgxmit_uctdprblmwl_z_n rgctdprblmwl \
   ltcdmi ss2cr12_n     xbmuxff2dh2s
```

Don't know how this happened or what to fix.

Fred.

.

From: tbr

Sent: Monday, December 19, 1994 7:54 PM

To: 'fwo (Fred Obermeier)'

Cc: 'fwo'; 'mws'

Subject: Re: More euterpe csyn errors.

Follow Up Flag: Follow up

Flag Status: Red

Fred Obermeier wrote (on Mon Dec 19):

Mark and I poked around a bit more.

We looked for the signal, rgxmit_uctdprblmwl_z.
The ~/chip/proteus/verilog/mlib/dandff2_1.v cell does indeed use a xbc01
generator, but my generated netlist, tbr_euterpe-pass1.splvs, doesn't connect
this cell to a 0/1 generator:

```
xrgxmituctdprblmwlu0    vii6 phi_a2p phi_b2p phi_a2p phi_b2p rgctdprblmwl_n \
   vrr6_2 vrr6_1 vrr6_0 ltcdmissvldr12 ltcdmissvldr12_n
  + rgxmit_uctdprblmwl_z ltcdmiss2cr12 rgxmit_uctdprblmwl_z_n rgctdprblmw! \
   ltcdmi ss2cr12_n      xbmuxff2dh2s
```

Don't know how this happened or what to fix.

I think the next place to look is in the edif file. As far as I can
see, the verilog for dandff2_1 is fine and the c01 is connected up.
Indeed if it were't I doubt we could simulate anything.

Tim

```
>It still fits.
```

Oh, happy day.

```
>Fix cc->nb timing problems.
```

OK, will do.

billz

Geert Rosseel wrote (on Tue Dec 20):

        ****
         NEW STUFF   (TO BE RELEASED IN /U/CHIP BY TONIGHT)
        ****
        2. hc0 : make higher and narrower
                    X origin same as before
                    YMIN = 437 (it will start right above dr)
                    YMAX = 665 (last usable row = 665 : same as before)
                    Jay

I am in the middle of a performance fix and I am not ready to release at this point.

        6. Place latest uu. Use latest uu.power.tab.top.
           uu cannot extend beyond the third clock spar from the left.
                    Jay

Nothing new has been checked in since last build. The snap shot just needs to use the uu.power.tab.top.

Jay

From: brianl (Brian Lee)
Sent: Tuesday, December 20, 1994 1:18 PM
To: 'Geert Rosseel'
Subject: Re: Euterpe status

Geert Rosseel writes:

> **************
> STUFF FROM YESTERDAY (TO BE DONE BY NOON TODAY) :
> **************
>
>   3. Cut 3 rows from the top from sr
>   and move sr down with 1 row.
>   Brianl

Unfortunately, taking out those 3 rows wasn't very straightforward. I had to rip out a lot of custom sections. I'm in the middle of a local build now ... hopefully it will work. If it does, I will release it.

I also didn't remember to change my local obstacles so that it would add an extra row at the bottom. However, I don't think that the extra row is needed anyways. The y-offset will be 420 instead of 419.

--
    Brian L.

Geert Rosseel writes:

> 3. Cut 3 rows from the top from sr
>   and move sr down with 1 row.
>   Brianl

Well, it is not finished yet and it seems to be having trouble making timing, but I'm releasing it anyways so that you at least have something that fits better ... hopefully.

I will try to salvage some of the custom pieces that I threw out in hopes getting a better placement.

--
   Brian L.

From: geert (Geert Rosseel)

Sent: Wednesday, December 21, 1994 12:21 PM

To: 'billz'; 'brianl'; 'dickson'; 'mws'; 'tbr'; 'vo'; 'woody'

Subject: Euterpe Meeting

Hi,

Can we meet at 2:00 p.m. today to discuss the Euterpe status ?

    Geert

From: doi (Derek Iverson)
Sent: Wednesday, December 21, 1994 1:14 PM
To: 'sandeep'; 'quarino'; 'jerry'; 'gmo'; 'jeffm'; 'iimura'; 'wayne'
Cc: 'hestia'
Subject: Software Bringup Meeting Minutes - December 21, 1994

Software Bringup Meeting

            December 21, 1994

Next Meeting: January 11 at 10:00 am.

Attendees: jeffm, guarino, doi, sandeep

Note: If there is any note-worthy activity between now and
             January 11, send email to the group.

New Action Items

-

Item: Run dcacheharder test and get cycle count results.
Who: doi
Status: [12/21] New.

Review of Action Items

Item: Implement parallel port device driver for Lynix on PC.
Who: jerry, doi
Status: [12/14] In progress.

Item: Get cycle counts of kernel tests to jeffm
Who: guarino
Status: [12/14] No progress.

Item: Define and implement a snapshot environment for the HW and SW
      simulators.
Who: jeffm, gmo
Status: [11/30] In progress

      Jeff is almost done summarizing his initial thoughts on the subject.

Item: Continue trying to find either source code for parallel drivers
      or descriptions of hardware so we can write out own.
Who: gmo   sgi machines
Who: doi   sun machines
Status: [11/23] progress continues (although not much).

      Expect info about Sun drivers from Acclaim (still).
      Expect info about SGI drivers from another vendor (still).
      Wayne says that National does not provice source for Suns but
      does for PCs and Macs.

Item: Build scripting/UI capabilities above gdb for regression tests.
Who: doi
Status: on hold until the the boot, gdb boot stub, and virtual devices
      are complete. (estimated start date of 1/10)

```
Item: Create performance test plan
Who:  jeffm, guarino
Status:      [11/30] In progress.

     Jeff sent out initial e-mail and the review process has started.

Item: Add Unix-like tests to software acceptance tests.
Who:  iimura
Status:      [11/30] In progress.

     Wally still investigating why the unix kernel is having problems
     booting multi-user with cycle counting enabled on terp.

Item: Simulator needs to understand `reset'
Who:  gmo
Status:      [11/30] In progress.

Item: Implement and bring-up boot, gdb boot stub, and virtual device
     support on the software simulator.
Who:  sandeep/gmo
Status:      in progress (delayed until 1/10 from original target of 12/23)

     On track.


Completed Items
-----------------------------------------------------------------------------
---

Item: Get cycle counts/differences for the oc-mem tests that lisar ran.
Who:  doi
Status:      [12/14] Done.

     Cycle counts were recorded for gtlb, {itag,ibuf,dbuf}_storeeasy
     instead of oc-mem since they were shorted tests that would allow
     for easier analysis of the results.


Test Status
-----------------------------------------------------------------------------
-

New zycad model should be built today to test uncached ifetch and nb load use bug fix.

Sync ops are being worked on now.
```

From:	yves (Jean-Yves Michel)
Sent:	Wednesday, December 21, 1994 4:25 PM
To:	'graham'; 'tony'; 'jt'; 'hessam'
Cc:	'pandora'
Subject:	RE: Euterpe housing containing Calliope

```
> From graham Wed Dec 21 13:31:47 1994
> Date: Wed, 21 Dec 1994 13:31:43 -0800
> From: graham (Graham Y. Mostyn)
> To: graham@charybdis, tony@charybdis
> Subject: RE: Euterpe housing containing Calliope
> Cc: yves, hessam, jt
> Content-Length: 807
>
> Re: the "first-out" minimal interface Calliope:
> I suggest that we might consider various combinations that could have
> market appeal; these are intended to fit in the Euterpe brick size,
> and be low risk (other than d).
>
> (a) I interpreted your email to suggest just a Calliope with a generic
> digital port that supports various wireline options (and perhaps other
> functions).  We would need to consider how the wireline electronics
> might be packaged; perhaps a set of additional same-size bricks that
> also fit in the rack, one for 3xISDN, one for T1 etc.??
```

That does not make too much sense: instead of designing 2 different bricks (1. calliope +
ISDN, 2. calliope + T1), we will be designing 3 bricks (1. calliope, 2. ISDN, 3. T1) with
all the extra costs : mechanical, power supply, board, connector ...

There are some limits to modularity. Each time we add a level of modularity, we add in
development cost, production cost and very often we get a performance hit.

```
> (b) Audio and NTSC video only.
>
> (c) Audio and RGB (metal change required for monitor quality)
```

I don't think calliope can sustain any high quality RGB. What about EGA or CGA?

```
>
> (d) RF interface only, eg cable receive. (Use with module b, or with
> PCI and monitor.)
>
> (e) possibilities for smart card reader, or IR transceiver?
> Graham.
>
```

For (b), (c) and (d), I suppose that Calliope resides also on each board otherwise we
would have analog signals on the backplane.
Then using (b) and (d) together as suggested, means 2 calliope.

Should not we develop an other form factor, a stepping stone instead
of a brick which would allow us to put all the I/Os on the
same board with enough room for all the connectors. Of course, the
complete
board will never be completed in time for early revenues, but we could
still sell it only partially populated, taylored to the application,
starting with low frequency I/O's.

Jean-Yves

From:	graham (Graham Y. Mostyn)
Sent:	Wednesday, December 21, 1994 5:24 PM
To:	'tony'; 'jt'; 'hessam'; 'yves'
Cc:	'pandora'
Subject:	RE: Euterpe housing containing Calliope

```
> From yves Wed Dec 21 14:25:06 1994
> Date: Wed, 21 Dec 1994 14:24:58 -0800
> From: yves (Jean-Yves Michel)
> To: graham, tony, jt, hessam
> Subject: RE: Euterpe housing containing Calliope
> Cc: pandora
> Content-Length: 2191
>
>
> > From graham Wed Dec 21 13:31:47 1994
> > Date: Wed, 21 Dec 1994 13:31:43 -0800
> > From: graham (Graham Y. Mostyn)
> > To: graham@charybdis, tony@charybdis
> > Subject: RE: Euterpe housing containing Calliope
> > Cc: yves, hessam, jt
> > Content-Length: 807
> >
> > Re: the "first-out" minimal interface Calliope:
> > I suggest that we might consider various combinations that could
> > have market appeal; these are intended to fit in the Euterpe brick
> > size, and be low risk (other than d).
> >
> > (a) I interpreted your email to suggest just a Calliope with a
> > generic digital port that supports various wireline options (and
> > perhaps other functions).  We would need to consider how the
> > wireline electronics might be packaged; perhaps a set of additional
> > same-size bricks that also fit in the rack, one for 3xISDN, one for
> > T1 etc.??
>
> That does not make too much sense: instead of designing 2 different
bricks
> (1. calliope + ISDN, 2. calliope + T1), we will be designing 3 bricks
> (1. calliope, 2. ISDN, 3. T1) with all the extra costs : mechanical,
> power supply, board, connector ...
>
> There are some limits to modularity. Each time we add a level of
> modularity, we add in development cost, production cost and very often
> we get a performance hit.
>
> > (b) Audio and NTSC video only.
> >
> > (c) Audio and RGB (metal change required for monitor quality)
>
> I don't think calliope can sustain any high quality RGB. What about
> EGA
or CGA?
>
> >
> > (d) RF interface only, eg cable receive. (Use with module b, or with
> > PCI and monitor.)
> >
> > (e) possibilities for smart card reader, or IR transceiver?
> > Graham.
> >
>
> For (b), (c) and (d), I suppose that Calliope resides also on each
> board otherwise we would have analog signals on the backplane.
```

> Then using (b) and (d) together as suggested, means 2 calliope.
>
>
> Should not we develop an other form factor, a stepping stone instead
> of a brick which would allow us to put all the I/Os on the same board
> with enough room for all the connectors. Of course, the
complete
> board will never be completed in time for early revenues, but we could
> still sell it only partially populated, taylored to the application,
> starting with low frequency I/O's.

I see the object as bringing the mixed signal technology to the marketplace early,
increasing revenues. Possibly an audio/video/ISDN combination, followed by sister
products that replace ISDN by T1, or FT1 etc., would optimize cost/value to the user, and
could be developed by us rapidly.

Graham.

>
> Jean-Yves
>

Hi,

Csyn has found errors in my latest build of tbr_euterpe-pass1.splvs in
/u/fwo/chip/euterpe/verilog/bsrc.

Could those reponsible for the following blocks make the appropriate changes?
Let me know when you have finished the fix so that I can retest euterpe.

Thanks,
Fred.

```
------------------------------------------------------------------
Absent Verilog Property Check:          SAME PROBLEM STILL EXISTS.
  This signal does not have a swing.  Try something like ckf_alpfw.

    missing legal node name from cell interface:
       cellname.pin  : ioff.ckf_alp
       cellname.pin  : ioff.ckf_b1p
------------------------------------------------------------------
Legal Leaf Cell Node Name Checks:
Floating Input Checks:                  I now have xbc01 generators, its
clean.
ADRS Correctness Check:                 I now have xbc01 generators, its
clean.
------------------------------------------------------------------
Output Shorts Check:                    We are now clean here.
------------------------------------------------------------------
Most Positive Voltage Check:        SAME PROBLEM STILL EXISTS.
   Cgeb is still a problem: 1p phi connects to other 2p signals: phi_a2p
        leaf connections:
        ...
          instance path:  top.xclk        .xu103u103.ckrbo_ad1ph
        cellname path:  top.cgclockbias.cgeb      .ckfo_ad1phw
        ...
        instance path:  top.xio0ursou3.philwest_a2p
        cellname path:  top.scsynch11 .phi_a2p
        ...

    Other similar leaf connections that should be 2p:
        instance path:  top.xclk        .xu103u103.ckrbo_bd1ph
        cellname path:  top.cgclockbias.cgeb      .ckfo_bd1phw

        instance path:  top.xclk        .xu102u105.ckrao_ad1ph
        cellname path:  top.cgclockbias.cgeb      .ckfo_ad1phw

        instance path:  top.xclk        .xu102u105.ckrao_bd1ph
        cellname path:  top.cgclockbias.cgeb      .ckfo_bd1phw
------------------------------------------------------------------
Single Input Swing Check:           We are now clean.
Exclusive Input Set Check:
Exclusive Input Swing Check:
Differential Input Pair Check:
------------------------------------------------------------------
Differential Input Swing Check:
    Due to a problem with the logic0/logic1 differential rule,
    there are a lot of false failures.  All reported errors appear to be
    logic0/logic1 related.  So I think we're clean here.
------------------------------------------------------------------
```

From: vo (Tom Vo)
Sent: Thursday, December 22, 1994 11:06 AM
To: 'geert (Geert Rosseel)'
Subject: xlu in chip

The build completed , but the atom count is larger than the one in :

/n/ghidra/s4/vo/lisar/euterpe/verilog/bsrc/xlu .

I'm puzzled .

tvo

From:	mws (Mark Semmelmeyer)
Sent:	Thursday, December 22, 1994 2:03 PM
To:	'lisar'; 'woody'
Cc:	'tbr'; 'geert'
Subject:	Re: ltlb X CORRUPT

BOM 196 is release. It does not have dickson's latest cc & euterpe.V because they were not locally released.
I assumed that woody's running a test covered for me running.

From:	tbr
Sent:	Thursday, December 22, 1994 3:34 PM
To:	'tom (Tom Laidig)'
Cc:	'cadettes@MicroUnity.com'; 'lisar'; 'tom (Thomas Laidig)'; 'Kurt Wampler'
Subject:	Re: License daemon status (fwd)
Follow Up Flag:	Follow up
Flag Status:	Red

Tom Laidig wrote (on Wed Dec 21):

I note also that the license for VXI-Logic will expire 31-dec-94, which
is pretty soon. Do we need to renew this?

Yes, urgently. Without that euterpe verification will stop.

Tim

From:	tbr
Sent:	Thursday, December 22, 1994 3:57 PM
To:	'geert'
Cc:	'tom'
Subject:	snapshot full
Follow Up Flag:	Follow up
Flag Status:	Red

Have you changed the Makefile so as not to clean up the gards
sub-dir after a successful build in a sub-block?

The euterpe-snapshot area has filled up and it appears to be because
none of the intermediate files in the gards dirs have been deleted.

Tim

From: tbr (Tim B. Robinson)
Sent: Thursday, December 22, 1994 3:58 PM
To: 'geert'
Cc: 'tom'
Subject: snapshot full

Have you changed the Makefile so as not to clean up the gards sub-dir after a successful build in a sub-block?

The euterpe-snapshot area has filled up and it appears to be because none of the intermediate files in the gards dirs have been deleted.

Tim

page from chip to geert:
Release euterpe/verilog/bsrc BOM 197.0 initiated by mws completed @ Thu Dec 22 14:28:24
PST 1994 with exit status 0.. chip

From: lisar (Lisa Robinson)

Sent: Friday, December 23, 1994 9:48 AM

To: 'jeffm'; 'woody'

Cc: 'billz'; 'dickson'; 'mws'; 'tbr'

Subject: BOM 197

The fix fixed ltlb but unfortunately didn't ge the others. I ran memtest
yesterday in verilog but forced on chip and it fabbed!

I've put tham back on the queue with a likedriverlog in
/s2/euterpe/verilog/bsrc/res/231294.7854 .... at high priority

Jeff you will have to run the verify ....

       Design Name: c_euterpe_wrap
       Run Date: 231294
       Run ID: 28537

Simulator: c_euterpe_wrap.mif.mm was built on Fri Dec 23 0:07:25 1994

Using BOM: Version BOM,v 197.0 1994/12/22 14:22:58 LT mws
Warning: Local BOM is out of date ...
Latest BOM is: RCS Version: No revision control file
Warning: Local BOM differs from that used to build c_euterpe_wrap.mif.mm

Log Message:
Run started on host: aphrodite at: Fri Dec 23 00:12:03 PST 1994

      store_unique_0   (in fail loop) Failed
        memtest_0   (in fail loop) Failed
          ltlb_0   Ran ok
      dcacheeasy_0   Ran ok
       exfixeasy_0   (in fail loop) Failed
      exresmajor_0   (looks like X's) Failed

Lisa R.

From: lisar (Lisa Robinson)

Sent: Friday, December 23, 1994 10:17 AM

To: 'tbr'

Cc: 'jeffm'

Subject: ikos flashrom

Doesn't work. The following traces are in /n/rhodan/s3/euterpe/verilog/bsrc/res/pass.run/results.

test1_0.dpo - likedriverlog.sig, strobed
test1_0.rom - rom.sig strobed
test1_0.rom.all - rom.sig all transitions

The script is pass.run and it runs test1 only. It doesn't record rom.sig.

Lisa R.

Tim, Geert,

I'd like to have a meeting and discuss the implications of the thermal dissipation of the CMOS Euterpe. Herman has put together some calculations and estimates of junction temperature for various solutions. How about this morning around 11am?

Thanks,
-jt

John Tang   Internet: jt@microunity.com
MicroUnity Systems Engineering, Inc.
255 Caspian Dr. Sunnyvale, CA 94089
(408)734-8100, (408)734-8177 fax

From: geert (Geert Rosseel)

Sent: Friday, December 23, 1994 11:50 AM

To: 'geert@MicroUnity.com'; 'jt@MicroUnity.com'; 'tbr@MicroUnity.com'

Cc: 'hchu@MicroUnity.com'; 'tbe@MicroUnity.com'

Subject: Re: CMOS Euterpe heat

11:00 a.m. is good for me ...

    Geert

From: lisar (Lisa Robinson)

Sent: Friday, December 23, 1994 12:04 PM

To: 'dickson'; 'jeffm'; 'tbr'; 'woody'

Subject: Likedriverlog traces

Of store_unique_0,memtest_0 and exfixeasy_0 are in

/n/nosferatu/s2/euterpe/verilog/bsrc/res/231294.7854/results/*.dpo

Lisa R.

A qick glance at the store test seems to imply that little endian 32 bit stores are broken.
They are picking off the top 32 bits not the bottom.

```
>From William Herndon ...
@
@
@ > From ong Thu Dec 22 10:19:21 1994
@ > From: ong (Warren R. Ong)
@ > Subject: Re: Update on csyn results
@ > To: fwo@ares.microunity.com (Fred Obermeier) @ > Date: Thu, 22 Dec 94 10:18:57 PST @ >
Cc: hardheads, fwo (Fred Obermeier) @ > X-Mailer: ELM [version 2.3 PL11] @ > Content-
Length: 1382 @ > @ > >From Fred Obermeier ...
@ > @
@ > @ Hi,
@ > @
@ > @ Csyn has found errors in my latest build of tbr_euterpe-pass1.splvs @ > @ in
/u/fwo/chip/euterpe/verilog/bsrc.
@ > @
@ > @ Could those reponsible for the following blocks make the appropriate changes?
@ > @ Let me know when you have finished the fix so that I can retest euterpe.
@ > @
@ > @ Thanks,
@ > @ Fred.
@ > @
@ > @
-----------------------------------------------------------------------
@ > @ Absent Verilog Property Check:          SAME PROBLEM STILL EXISTS.
@ > @    This signal does not have a swing.  Try something like ckf_a1pfw.
@ > @
@ > @      missing legal node name from cell interface:
@ > @         cellname.pin  : ioff.ckf_a1p
@ > @         cellname.pin  : ioff.ckf_b1p
@ > @
-----------------------------------------------------------------------
@ >
@ > < snip >
@ >
@ > This subcircuit (ioff) and the custom block that uses this @ > subcircuit (iobyte)
previously passed csyn & celltest.  Something has @ > changed in csyn or celltest to
render "ckf_[ab]1p" a non valid @ > clock signal.  Note that this signal is a non-standard
clock @ > signal that is shifted 1p (not 2p down).  It use to be in the @ > signame
registry.  Does celltest know to treat these as clock inputs?
@ >
@ > Changing this signal name will affect the following areas:
@ >
@ > Schematics:
@ >    ioff
@ >    ioffload
@ >    ioquadctrl (if interface pin of ioffload is changed as well)
@ >    iobyte0
@ >
@ > Layout:
@ >    ioff.ly
@ >
@ > Verilog:
@ >    ioff.v
@ >
@ > Do we really want to make this change?
@ >
@ > --
@ >          Warren.
```

```
@ >
@
@ Warren, maybe you can shed some light on this.. when fwo and kurt looked at this they
were @ alarmed that there was too much load on a clock buffer even if a lp signal was ok..
@ a clock buffer should be able to tolerate something like 300 - 600ff total load. if we
are @ below 300ff we are ok @
```

Are we talking about the same clock signal? This particular signal is driven from the
quadrature circuit and is internal to iobyte. Or are you referring to a signal on iobyte
called "phio_[ab]d2ph"?

```
--
```

        Warren.

From: tbr

Sent: Friday, December 23, 1994 11:22 PM

To: 'geert'

Subject: Makefile problem

Follow Up Flag: Follow up

Flag Status: Red

I have the latest Makefile.defs and Makefile.rules, and I am on BOM
197.0 of euterpe. When I try to run the gards for io0 it dies on
pass2 with:

```
#
# Get an initial sdl file.  A manhattan approximation will be used
#
gmake  CYCLETIME=895 gards/io0-pass2.sdl
gmake[2]: Entering directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/io'
gmake[2]: `gards/io0-pass2.sdl' is up to date.
gmake[2]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/io'
#
# Now route it - can't ask for this directly because gplace rule would
# be needed twice.  gmake forbids this
#
gmake  CYCLETIME=895 gards/io0-pass2.garout.lis
gmake[2]: Entering directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/io'
gmake[2]: *** No rule to make target `gards/io0-pass2.garout.lis'.  Stop.
gmake[2]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/io'
gmake[1]: *** [io0-base.short.nets] Error 1
gmake[1]: Leaving directory `/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/io'
gmake: *** [io0gards] Error 1
```

Any idea whats missing?

Tim

I have the latest Makefile.defs and Makefile.rules, and I am on BOM 197.0 of euterpe.
When I try to run the gards for io0 it dies on
pass2 with:

```
#
# Get an initial sdl file.  A manhattan approximation will be used # gmake  CYCLETIME=895
gards/io0-pass2.sdl
gmake[2]: Entering directory
`/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/io'
gmake[2]: `gards/io0-pass2.sdl' is up to date.
gmake[2]: Leaving directory
`/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/io'
#
# Now route it - can't ask for this directly because gplace rule would # be needed twice.
gmake forbids this # gmake  CYCLETIME=895 gards/io0-pass2.garout.lis
gmake[2]: Entering directory
`/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/io'
gmake[2]: *** No rule to make target `gards/io0-pass2.garout.lis'.  Stop.
gmake[2]: Leaving directory
`/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/io'
gmake[1]: *** [io0-base.short.nets] Error 1
gmake[1]: Leaving directory
`/N/auspex/root/s15/tbr/euterpe/verilog/bsrc/io'
gmake: *** [io0gards] Error 1
```

Any idea whats missing?

Tim

From: geert (Geert Rosseel)

Sent: Saturday, December 24, 1994 12:13 PM

To: 'euterpe-checkins-dist'; 'lisar'; 'tbr'; 'tom'

Subject: euterpe/verilog/bsrc/ife ife_control.pim

Update of /u/chip/chip-archive/euterpe/verilog/bsrc/ife
In directory staypuft:/N/auspex/root/s41/euterpe-snapshot/euterpe/verilog/bsrc/ife

Modified Files:
      ife_control.pim
Log Message:
Updated placement

Geert

From: hopper (Mark Hofmann)

Sent: Monday, December 26, 1994 7:10 AM

To: 'Tim B. Robinson'

Cc: 'tom (Thomas Laidig)'; 'lisar (Lisa Robinson)'; 'ken (Ken Hsieh)'

Subject: Re: License daemon status (fwd)

Tim B. Robinson writes:

Tom Laidig wrote (on Wed Dec 21):

I note also that the license for VXI-Logic will expire 31-dec-94, which
is pretty soon. Do we need to renew this?

Yes, urgently. Without that euterpe verification will stop.

Ugh. We've gotta get this stuff in order. It's a mess. Part of the problem
is that this VXI tool is being traded from Sim Tech to Zycad. So, do I have
this right, we need and are using:

/a/license/license.vxi.1.1.combined

```
SERVER rhea 55000dbe 5220
DAEMON stld /a/vxi/vxi_1.1/license/stld_vxi
FEATURE VXI-Base stld 2.000 1-feb-95 1 1B78805118BB13A4482A "" 5540951e
FEATURE VXI-XFault stld 1.100 31-dec-99 1 1B88D091D111C28E0F9C "SimTech" 5540951e
FEATURE VXI-Base stld 2.000 1-feb-95 1 FB18E0F130ED4C0C78FF "" 55419dea
FEATURE VXI-XFault stld 1.100 31-dec-99 1 5BE840F17001526AE0A2 "SimTech" 55419dea
FEATURE VCD+ stld 1.200 16-sep-94 5 0BBC0ED256BE1B873680 "SimTech"
FEATURE VirSim-Base stld 1.200 16-sep-94 5 DBEC9E32BB05BABF9711 "SimTech"
FEATURE VirSim-Source stld 1.200 16-sep-94 5 AB3C0E02C31624140953 "SimTech"
FEATURE VirSim-Logic stld 1.200 16-sep-94 5 CB4C0E729B5F52025C4F "SimTech"
```

And, also:

/a/zycad/license/license.dat

```
SERVER aphrodite 5540951e 1799
DAEMON ZYCADD /a/zycad/license/zdaemon
FEATURE xplusC ZYCAD 5 12-jan-94 1 7CA26135703377C5 "700" 5540951e
FEATURE xplusC ZYCAD 5 12-jan-94 1 30929FF474FFA0AD "700" 55419dea
FEATURE VM ZYCADD 3.000 13-dec-95 1 7B89877FCE132B4021E2 "" 5540951e
FEATURE VXI-Logic none 1.000 31-dec-94 0 CB18D0B1C62650C97184 "Simulation Technologies, (C) 1992" 55419dea
FEATURE VXI-Logic none 1.000 31-dec-94 0 0B18C061785B52C31CF7 "Simulation Technologies, (C) 1992" 5540951e
```

Except that we are _not_ making use of the xplusC stuff.
[We did get a new license file (which Ken installed), but it seems to
only have update the ZYCAD demon and not the software.]

It sounds like Zycad needs to issue us a new VXI-Logic license. We should
then attempt to combine this license file with the rest of the VXI stuff
and store it in the /a/license area.

I will contact Zycad Tuesday, 27 Dec.

-hopper

From:	tbr
Sent:	Tuesday, December 27, 1994 11:55 AM
To:	'lisar (Lisa Robinson)'
Cc:	'jeffm'
Subject:	ikos flashrom
Follow Up Flag:	Follow up
Flag Status:	Red

Lisa Robinson wrote (on Fri Dec 23):

Doesn't work. The following traces are in /n/rhodan/s3/euterpe/verilog/bsrc/res/pass.run/results.

test1_0.dpo - likedriverlog.sig, strobed
test1_0.rom - rom.sig strobed
test1_0.rom.all - rom.sig all transitions

The script is pass.run and it runs test1 only. It doesn't record rom.sig.

There is no group write in bsrc, so I can't run it as me. I'll be you
for a while . . .

Tim

From:	tbr
Sent:	Tuesday, December 27, 1994 11:58 AM
To:	'lisar'
Subject:	s3/bsrc
Follow Up Flag:	Follow up
Flag Status:	Red

Still can't run as you:

43   system date
Tue Dec 27 09:56:54 PST 1994
44   elaborate -p i_euterpe_wrap_tbw -s tb
Collector: cannot find library unit "dls_work.i_euterpe_wrap_tbw(tb)".
    Try reanalyzing the library unit.
Error: current operation terminated due to interrupt or FATAL error.
elaborate: Error Tsvc::ChildHadError
Please re-elaborate the design

What's the status here?

Tim

Had now problem. Did you set dls_work correctly?

Note I moved the original res/pass.run to res/pass.run.1.

Lisa R.
lisar@rhodan /s3/euterpe/verilog/bsrc 444 % mv res/pass.run res/pass.run.fail
lisar@rhodan /s3/euterpe/verilog/bsrc 445 % ikos
lisar@rhodan /s3/euterpe/verilog/bsrc 446 % setenv dls_work `abspath`/.cs_dir
lisar@rhodan /s3/euterpe/verilog/bsrc 447 % vsh -X
Voyager System Software 2.00L CS/CSX Oct 17 1994
Copyright 1991-1994 IKOS Systems Inc., Cupertino, CA.

IVSP_20008 installed Dec 02 1994
vsh% source pass.run
```
1      -- A vsh script
2      setvar simulator CSX-Nsim
3      --setvar simulator CS
4      setvar startisis TRUE
5      setvar resunits 50
6      setvar resbase ps
7
8      --
sh /u/chip/tools/vendor/ikos/voyager_2.0/bin/sun_sparc/analyze /n/rhodan/s3/euterpe/verilog/bsrc/i_euterpe_wrap.vhdl
9      --sh /u/chip/tools/vendor/ikos/voyager_2.0/bin/sun_sparc/analyze /n/rhodan/s3/euterpe/verilog/bsrc/i_euterpe_wrap.tb
10
11
12     sh  mkdir res/pass.run
13     sh  chmod 777 res/pass.run
14     sh  mkdir res/pass.run/vectors
15     sh  chmod 777 res/pass.run/vectors
16     sh  mkdir res/pass.run/logfiles res/pass.run/results
17     sh  chmod 777 res/pass.run/logfiles res/pass.run/results
18     sh  echo 'Log Message:  '>> res/pass.run/logfiles/cdate
19     sh  cp ../../verify/config/cerb.hdr .//cerb.in
20     sh  cat ../../verify/toplevel/./test1_0.in >> cerb.in
21     sh  cp ../../verify/config/cie.hdr .//cie.in
22     sh  cat ../../verify/toplevel/./test1_0.cie >> cie.in
23     sh  cp ../../verify/config/cio.hdr .//cio.in
24     sh  cat ../../verify/toplevel/./test1_0.cio >> cio.in
25     sh  cp ../../verify/config/cde.hdr .//cde.in
26     sh  cat ../../verify/toplevel/./test1_0.cde >> cde.in
27     sh  cp ../../verify/config/cdo.hdr .//cdo.in
28     sh  cat ../../verify/toplevel/./test1_0.cdo >> cdo.in
29     sh  cp ../../verify/config/ctd.hdr .//ctd.in
30     sh  cat ../../verify/toplevel/./test1_0.ctd >> ctd.in
31     sh  cp ../../verify/config/cti.hdr .//cti.in
32     sh  cat ../../verify/toplevel/./test1_0.cti >> cti.in
33     sh  cp ../../verify/config/dram.hdr .//dram.in
cp: ../../verify/config/dram.hdr: No such file or directory
34     sh  cat ../../verify/toplevel/./test1_0.dram >> dram.in
```

```
35     sh  cp ../../verify/config/rom.hdr .//rom.in
cp: ../../verify/config/rom.hdr: No such file or directory
36     sh  cat ../../verify/toplevel/./test1_0.rom >> rom.in
37     sh  cp ../../verify/toplevel/./test1_0.bs .
38     sh  cp ../../verify/toplevel/./test1_0.wav .
39     sh  cp ../../verify/toplevel/./test1_0.inp .
40     sh  cp ../../verify/toplevel/./test1_0.slr .
41     sh  cp ../../verify/toplevel/./test1_0.sig .
42     stimxl -c 0 eu.bs
43     system date
Tue Dec 27 10:36:09 PST 1994
44     elaborate -p i_euterpe_wrap_tbw -s tb
Collecting units for design: dls_work.i_euterpe_wrap_tbw(tb)
   dls_work.i_euterpe_wrap_tbw(tb)
   dls_std.standard
   dls_std.foreign
   dls_ieee.std_logic_1164
   dls_ieee.std_logic_1164(body)
   dls_work.i_euterpe_wrap_tbw
   dls_work.i_euterpe_wrap
   dls_work.i_euterpe_wrap(gates)


Elaborating simulator "nsim-hardware"...
warning [18000058,6]: cf_everead:  No host assigned to IOU 001
in /u/chip/tools/vendor/ikos/voyager_2.0/admin/rhodan_nsim0/rhodan_nsim0.simcfg.
Installing gate level netlist...
Installing gate level memory patterns...
Finished connecting signals to simulator "nsim-hardware"
Annealing design in simulator 'nsim-hardware'...
Annealing complete.
45     source ../../verify/config/i_euterpe_wrap.parm
1      installmem -p cerb.in -f u /uut/stimu/u110/core
rom -i /s3/euterpe/verilog/bsrc/cerb.in -w 152 -l -f U -o /s3/euterpe/verilog/bsrc/cerb.l_152_U.crm -e /usr/tmp/rom.errdb
initializing
the rom compiler options are:
input file name  = /s3/euterpe/verilog/bsrc/cerb.in
output file name = /s3/euterpe/verilog/bsrc/cerb.l_152_U.crm
error file name = /usr/tmp/rom.errdb
wordsize       = 152
the pattern is little ending
fill pattern is undefines
starting to process /s3/euterpe/verilog/bsrc/cerb.in

initializing
starting to process /s3/euterpe/verilog/bsrc/cerb.in
opening /s3/euterpe/verilog/bsrc/cerb.l_152_U.crm!
roms are compiled
Installing gate level memory patterns...
2      installmem -p cie.in -f u /uut/euterpe/ci/blockl/core
rom -i /s3/euterpe/verilog/bsrc/cie.in -w 64 -l -f U -o /s3/euterpe/verilog/bsrc/cie.l_64_U.crm -e /usr/tmp/rom.errdb
initializing
the rom compiler options are:
input file name  = /s3/euterpe/verilog/bsrc/cie.in
output file name = /s3/euterpe/verilog/bsrc/cie.l_64_U.crm
error file name = /usr/tmp/rom.errdb
wordsize       = 64
the pattern is little ending
fill pattern is undefines
starting to process /s3/euterpe/verilog/bsrc/cie.in

initializing
```

starting to process /s3/euterpe/verilog/bsrc/cie.in
opening /s3/euterpe/verilog/bsrc/cie.1_64_U.crm!
roms are compiled
Installing gate level memory patterns...
3   installmem -p cio.in -f u /uut/euterpe/ci/blockh/core
rom -i /s3/euterpe/verilog/bsrc/cio.in -w 64 -l -f U -o /s3/euterpe/verilog/bsrc/cio.1_64_U.crm -e /usr/tmp/rom.errdb
initializing
the rom compiler options are:
input file name = /s3/euterpe/verilog/bsrc/cio.in
output file name = /s3/euterpe/verilog/bsrc/cio.1_64_U.crm
error file name = /usr/tmp/rom.errdb
wordsize   = 64
the pattern is little ending
fill pattern is undefines
starting to process /s3/euterpe/verilog/bsrc/cio.in

initializing
starting to process /s3/euterpe/verilog/bsrc/cio.in
opening /s3/euterpe/verilog/bsrc/cio.1_64_U.crm!
roms are compiled
Installing gate level memory patterns...
4   installmem -p cde.in -f u /uut/euterpe/cd/blockl/core
rom -i /s3/euterpe/verilog/bsrc/cde.in -w 64 -l -f U -o /s3/euterpe/verilog/bsrc/cde.1_64_U.crm -e /usr/tmp/rom.errdb
initializing
the rom compiler options are:
input file name = /s3/euterpe/verilog/bsrc/cde.in
output file name = /s3/euterpe/verilog/bsrc/cde.1_64_U.crm
error file name = /usr/tmp/rom.errdb
wordsize   = 64
the pattern is little ending
fill pattern is undefines
starting to process /s3/euterpe/verilog/bsrc/cde.in

initializing
starting to process /s3/euterpe/verilog/bsrc/cde.in
opening /s3/euterpe/verilog/bsrc/cde.1_64_U.crm!
roms are compiled
Installing gate level memory patterns...
5   installmem -p cdo.in -f u /uut/euterpe/cd/blockh/core
rom -i /s3/euterpe/verilog/bsrc/cdo.in -w 64 -l -f U -o /s3/euterpe/verilog/bsrc/cdo.1_64_U.crm -e /usr/tmp/rom.errdb
initializing
the rom compiler options are:
input file name = /s3/euterpe/verilog/bsrc/cdo.in
output file name = /s3/euterpe/verilog/bsrc/cdo.1_64_U.crm
error file name = /usr/tmp/rom.errdb
wordsize   = 64
the pattern is little ending
fill pattern is undefines
starting to process /s3/euterpe/verilog/bsrc/cdo.in

initializing
starting to process /s3/euterpe/verilog/bsrc/cdo.in
opening /s3/euterpe/verilog/bsrc/cdo.1_64_U.crm!
roms are compiled
Installing gate level memory patterns...
6   installmem -p cti.in -f u /uut/euterpe/cti/word0/core
rom -i /s3/euterpe/verilog/bsrc/cti.in -w 64 -l -f U -o /s3/euterpe/verilog/bsrc/cti.1_64_U.crm -e /usr/tmp/rom.errdb
initializing
the rom compiler options are:
input file name = /s3/euterpe/verilog/bsrc/cti.in
output file name = /s3/euterpe/verilog/bsrc/cti.1_64_U.crm

error file name = /usr/tmp/rom.errdb
wordsize   = 64
the pattern is little ending
fill pattern is undefines
starting to process /s3/euterpe/verilog/bsrc/cti.in

initializing
starting to process /s3/euterpe/verilog/bsrc/cti.in
opening /s3/euterpe/verilog/bsrc/cti.l_64_U.crm!
roms are compiled
Installing gate level memory patterns...
7   installmem -p ctd.in -f u /uut/euterpe/ctd/word0/core
rom -i /s3/euterpe/verilog/bsrc/ctd.in -w 64 -l -f U -o /s3/euterpe/verilog/bsrc/ctd.l_64_U.crm -e /usr/tmp/rom.errdb
initializing
the rom compiler options are:
input file name = /s3/euterpe/verilog/bsrc/ctd.in
output file name = /s3/euterpe/verilog/bsrc/ctd.l_64_U.crm
error file name = /usr/tmp/rom.errdb
wordsize   = 64
the pattern is little ending
fill pattern is undefines
starting to process /s3/euterpe/verilog/bsrc/ctd.in

initializing
starting to process /s3/euterpe/verilog/bsrc/ctd.in
opening /s3/euterpe/verilog/bsrc/ctd.l_64_U.crm!
roms are compiled
Installing gate level memory patterns...
8   record -f ../../verify/toplevel/./test1_0.sig
9   record -f likedriverlog.sig
10   record -f ce_defaults.sig
11   system date
Tue Dec 27 10:39:53 PST 1994
12   run for 200000 ns

Starting simulator 'nsim-hardware' in Timing Mode...
Now 200000 ns   Events 0
13   system date
Tue Dec 27 10:40:45 PST 1994
14   --waves -hex -trace ce_defaults.sig
15   waves -hex -start 111000 -strobe 3ns 3ns 6ns -trace likedriverlog.sig -out res/pass.run/results/test1_0.dpo
vsh%

From: fwo (Fred Obermeier)
Sent: Tuesday, December 27, 1994 9:11 PM
To: 'bpw'; 'bpw@MicroUnity.com'; 'ong'
Cc: 'bill'; 'fwo'; 'hardheads'
Subject: Re: Celltest conditions update.

BPW,

I am glad that you have raised your concerns. It is through this process
that we improve our overall environment. In this case, I can better
understand what we all want celltest to do.

Design reviews are usually called to discuss the future direction
of projects. These are open to anyone with an interest in the area.
We haven't haven't got to the celltest part yet. I've instead made
improvements that follow a path of tighen voltage constraints and
passing criterion to help identify circuits with problems.

We have had a design review for the csyn part where substantial changes
were suggested. Some of these are quite urgent. Since csyn circuit
connectivity checks usually catch the majority of wiring errors,
most of my recent efforts have been focused on euterpe's csyn.
I'm sure we'll get to having a rewview celltest.

Thanks,
Fred.

BPW,

I am glad that you have raised your concerns. It is through this process that we improve our overall environment. In this case, I can better understand what we all want celltest to do.

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We haven't haven't got to the celltest part yet. I've instead made improvements that follow a path of tighen voltage constraints and passing criterion to help identify circuits with problems.

We have had a design review for the csyn part where substantial changes were suggested. Some of these are quite urgent. Since csyn circuit connectivity checks usually catch the majority of wiring errors, most of my recent efforts have been focused on euterpe's csyn. I'm sure we'll get to having a rewview celltest.

Thanks,
Fred.

From:	tbr
Sent:	Tuesday, December 27, 1994 5:14 PM
To:	'mudge'; 'anh'
Cc:	'lisar'
Subject:	Mnemosyne schedule
Follow Up Flag:	Follow up
Flag Status:	Red

We currently expect to be ready to ship masks for the MOBI version of
Mnemosyne on April 7, 95, though we are trying to pull that in a little.

For the top level Pandora schedule I need input on when we can expect
packaged tested parts given the above tapeout date. If you can let me
have a timeline with as much detail as you can include, lisar can
integrate this into the top level schedule. Since Mnemosyne will be
in the critical path to a working Pandora please give this your
careful attention ASAP.

Thanks
Tim

B. P. Wong writes:
    I was only wondering if there was a cheaper way of doing the kind of checks
    that we are using celltest for. Besides the bias generator for the resistor
    code compensates for the swing, therefore, the only failures due to swing
    is performance related. Other factors can also cause this kind of logical
    failures and we are not testing for but are just focusing on rcds.
Basically
    from what I gather from the recent emails is that celltest is a totally
    different tool from what it was when it was concieved.

Hopper jumps in:

   Celltest has certainly changed from its first beginnings. However, I think the intent is
still to be able to use the tool to verify both proper logical operation (as compared
against the Verilog simulation) and electrical performance (where the spice results are
compared against the qualifiers in each signal's name).

   The capabilities of Celltest have been expanded in an attempt to more automatically
verify some of the different operating conditions of the leaf circuits that it tests. I
agree that much more could be done then simply varying r-codes. Perhaps it is foolish to
fixate only on that one parameter, and neglect other (possibly more) gross effects. And
perhaps there is a lower CPU-cost way to check these corner cases. I'm not sure of that;
it seems that any such check would always involve a Spice simulation. The overhead for
managing these simulations (that Celltest imposes) is small compared to the simulation
runtime (and the benefit, I would argue, is great).

   The r-code tests are being put in principally to aid the automated generation and
testing of our 1500-odd leafcell library. Since we may want to run Euterpe at r-codes 1
through 7 it might be prudent to test the affected circuits at all r-codes. If a certain
custom circuit will never be run at a given r-code, it needn't be Celltested for that
case.

-hopper

From: hopper (Mark Hofmann)

Sent: Wednesday, December 28, 1994 5:30 AM

To: 'Ken Hsieh'

Cc: 'tbr (Tim B. Robinson)'; 'bpw (B. P. Wong)'

Subject: Re: frodo

Ken Hsieh writes:
  Hopper,

  Would you please give me a list of spice machine?
  I have no idea which of workstations have been defined as a spice
  machine.

Ken,

  Here is a list of all tools and licenses that I know about. This should
be filed somewhere (but I've forgotten where I put it!)

-hopper

```
Tool        Vendor       Demon  licensed nodes (arch)
--------    --------     -----  --------------
xpcad       altium       rhea   floats (sun)
gerberview  altium         rama  floats (sun)

allegro     cadence      rhea   floats (sun, hp)
caeviews    cadence        rhea  floats (sun, hp)
compile     cadence        rhea  floats (sun, hp)
concept     cadence        rhea  floats (sun, hp)
ged         cadence      rhea   floats (sun)
packager    cadence        rhea  floats (sun, hp)
verilog     cadence      rhea   floats (sun, hp)
v2e         cadence      none   aphrodite (sun)

dracula     cadence         on node tomato cyclops medusa mothra (sun)

xvlsi       compass      none   abderus euterpe kephalos millennium
                                poseidon ambiorix athena (sun)

vericheck   iss          hestia  tomato cyclops medusa mothra (sun)

energize    lucid        rhea   floats (sun)

hspice      meta-software  rhea  ambiorix ares boa frodo hera kephalos
                                mercury merope narcissus pegasus
                                pelorus phobos polyhymnia psyche thalia
gsi         meta-software  rhea  floats (sun, hp)

hyperplot   pinebush     none   godzilla (sun)

capclc      silver-lisco  godzilla floats (sun)
garout      silver-lisco  godzilla floats (sun)
gplace      silver-lisco  godzilla floats (sun)
maskout     silvar-lisco   godzilla floats (sun)
pcomp       silvar-lisco   godzilla floats (sun)
```

```
pgroute     silvar-lisco   godzilla floats (sun)
redit       silvar-lisco   godzilla floats (sun)
rdump       silvar-lisco   godzilla floats (sun)
rload       silvar-lisco   godzilla floats (sun)
slnet       silvar-lisco   godzilla floats (sun)


undertow     veritools     rhea   floats (sun)


edif22mif    zycad        none   nosferatu aphrodite (sun)
linkmm       zycad        none   nosferatu aphrodite (sun)
vxi          zycad        rhea   nosferatu aphrodite (sun)
virsim       zycad        rhea   floats
```

Vendor - License file Index:

Vendor: altium, tool: gerberview
License binary: /n/auspex/s34/ecam
License file: /n/auspex/s34/ecam/license.dat

Vendor: altium
License binary: /a/pcad/license/bin.sun4
License file: /a/pcad/license/pcadlic.dat

Vendor: cadence
License binary: /a/cadence/tools/bin
License file: /a/cadence/share/license/license.55000dbe

Vendor: cadence, tool: dracula
License binary: /a/dracula4.1/tools/bin
License file: /a/dracula4.1/share/license/license.55409301

Vendor: lucid
License binary: /s1/energize2.1/flexlm/bin   ???
License file: /s1/energize2.1/flexlm/etc/license.dat   ???

Vendor: silvar-lisco
License binary: /a/silvar-lisco/license
License file: /a/silvar-lisco/license/license.dat

Vendor: sun, tool: fortran compiler
License binary: /n/auspex/s34/fortran/license/bin4
License file: /n/auspex/s34/fortran/license/bin4/license.dat

Vendor: veritools
License binary: /a/veritools/Lic.Mgr+typetool/license
License file: /a/license/license.undertow

Vendor: zycad
License binary: /a/vxi/vxi_1.1/license
License file: /a/license/license.vxi.1.1.combined

From: bpw (B. P. Wong)
Sent: Wednesday, December 28, 1994 11:40 AM
To: 'fwo'
Cc: 'bill'; 'hardheads'
Subject: Re: Celltest conditions update.

> I am glad that you have raised your concerns. It is through this
process
> that we improve our overall environment. In this case, I can better
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>
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> passing criterion to help identify circuits with problems.
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> I'm sure we'll get to having a rewview celltest.
>
> Thanks,
> Fred.
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I was only wondering if there was a cheaper way of doing the kind of checks that we are
using celltest for. Besides the bias generator for the resistor code compensates for the
swing, therefore, the only failures due to swing is performance related. Other factors
can also cause this kind of logical failures and we are not testing for but are just
focusing on rcds.
Basically
from what I gather from the recent emails is that celltest is a totally different tool
from what it was when it was concieved.

bpw

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: generation and testing of our 1500-odd leafcell library. Since we may want
: to run Euterpe at r-codes 1 through 7 it might be prudent to test the affected
: circuits at all r-codes. If a certain custom circuit will never be run
: at a given r-code, it needn't be Celltested for that case.

Instead of running all the rcodes why not characterize one of the slowest circuit and find
the worst corner(or rcd in this case) then have celltest only run those rcds and may be a
few other codes as a reference.
This should allow celltest to get through all the 1500 leafcells in a timely fashion
instead of a blanket of extremely low return simulations.

bpw

B. P. Wong wrote (on Wed Dec 28):

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   : at a given r-code, it needn't be Celltested for that case.

   Instead of running all the rcodes why not characterize one of the slowest
   circuit and find the worst corner(or rcd in this case) then have celltest
   only run those rcds and may be a few other codes as a reference.
   This should allow celltest to get through all the 1500 leafcells in a
   timely fashion instead of a blanket of extremely low return simulations.

But missing just one case could be a killer. Unless I'm mistaken, the degree of
automation we now have means this is just a CPU time issue, not a human time issue, so we
should burn those cycles.

Tim

From:	tbr
Sent:	Wednesday, December 28, 1994 1:34 PM
To:	'ken'
Cc:	'hopper'; 'ericm'
Subject:	Re: frodo
Follow Up Flag:	Follow up
Flag Status:	Red

Please make sre as much of this as we can gets into eric's bones
database for future reference.

Tim

Mark Hofmann wrote (on Wed Dec 28):

Ken Hsieh writes:
Hopper,

Would you please give me a list of spice machine?
I have no idea which of workstations have been defined as a spice
machine.

Ken,

Here is a list of all tools and licenses that I know about. This should
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-hopper

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xpcad	altium	rhea	floats (sun)
gerberview	altium	rama	floats (sun)
allegro	cadence	rhea	floats (sun, hp)
caeviews	cadence	rhea	floats (sun, hp)
compile	cadence	rhea	floats (sun, hp)
concept	cadence	rhea	floats (sun, hp)
ged	cadence	rhea	floats (sun)
packager	cadence	rhea	floats (sun, hp)
verilog	cadence	rhea	floats (sun, hp)
v2e	cadence	none	aphrodite (sun)
dracula	cadence		on node tomato cyclops medusa mothra (sun)
xvlsi	compass	none	abderus euterpe kephalos millennium poseidon ambiorix athena (sun)
vericheck	iss	hestia	tomato cyclops medusa mothra (sun)
energize	lucid	rhea	floats (sun)
hspice	meta-software	rhea	ambiorix ares boa frodo hera kephalos

```
                    mercury merope narcissus pegasus
                    pelorus phobos polyhymnia psyche thalia
gsi         meta-software  rhea    floats (sun, hp)

hyperplot    pinebush       none   godzilla (sun)

capclc       silver-lisco   godzilla floats (sun)
garout       silver-lisco   godzilla floats (sun)
gplace       silver-lisco   godzilla floats (sun)
maskout      silvar-lisco   godzilla floats (sun)
pcomp        silvar-lisco   godzilla floats (sun)
pgroute      silvar-lisco   godzilla floats (sun)
redit        silvar-lisco   godzilla floats (sun)
rdump        silvar-lisco   godzilla floats (sun)
rload        silvar-lisco   godzilla floats (sun)
slnet        silvar-lisco   godzilla floats (sun)

undertow     veritools      rhea    floats (sun)

edif22mif    zycad          none   nosferatu aphrodite (sun)
linkmm       zycad          none   nosferatu aphrodite (sun)
vxi          zycad          rhea   nosferatu aphrodite (sun)
virsim       zycad          rhea   floats
```

Vendor - License file Index:

Vendor: altium, tool: gerberview
License binary: /n/auspex/s34/ecam
License file: /n/auspex/s34/ecam/license.dat

Vendor: altium
License binary: /a/pcad/license/bin.sun4
License file: /a/pcad/license/pcadlic.dat

Vendor: cadence
License binary: /a/cadence/tools/bin
License file: /a/cadence/share/license/license.55000dbe

Vendor: cadence, tool: dracula
License binary: /a/dracula4.1/tools/bin
License file: /a/dracula4.1/share/license/license.55409301

Vendor: lucid
License binary: /s1/energize2.1/flexlm/bin   ???
License file: /s1/energize2.1/flexlm/etc/license.dat   ???

Vendor: silvar-lisco
License binary: /a/silvar-lisco/license
License file: /a/silvar-lisco/license/license.dat

Vendor: sun, tool: fortran compiler
License binary: /n/auspex/s34/fortran/license/bin4
License file: /n/auspex/s34/fortran/license/bin4/license.dat

Vendor: veritools
License binary: /a/veritools/Lic.Mgr+typetool/license
License file: /a/license/license.undertow

Vendor: zycad
License binary: /a/vxi/vxi_1.1/license

License file: /a/license/license.vxi.1.1.combined

From: ken (Ken Hsieh)

Sent: Wednesday, December 28, 1994 1:51 PM

To: 'Tim B. Robinson'

Cc: 'hopper (Mark Hofmann)'; 'bpw (B. P. Wong)'; 'ericm (Eric Murray)'

Subject: Re: frodo

Tim,

The following is the swap space list of all spice machine which
defined on hopper's mail.

```
spice machine  swap space
------------  -----------
ambiorix          143 meg
ares          296 meg
frodo          511 meg
hera          328 meg
kephalos          235 meg
mercury          300 meg
merope          243 meg
narcissus          341 meg
pegasus          199 meg
pelorus          300 meg
phobos          328 meg
polyhymnia          300 meg
psyche         1036 meg
thalia          328 meg
boa        ???
```

frodo should have plenty of swap space.

ken
>
>
> Please make sre as much of this as we can gets into eric's bones
> database for future reference.
>
> Tim
>
> Mark Hofmann wrote (on Wed Dec 28):
>
>   Ken Hsieh writes:
>   Hopper,
>
>   Would you please give me a list of spice machine?
>   I have no idea which of workstations have been defined as a spice
>   machine.
>
>   Ken,
>
>   Here is a list of all tools and licenses that I know about. This should
>   be filed somewhere (but I've forgotten where I put it!)

```
> 
> -hopper
> 
> Tool          Vendor        Demon   licensed nodes (arch)
> --------      --------      -----   --------------
> xpcad         altium        rhea    floats (sun)
> gerberview    altium         rama   floats (sun)
> 
> allegro       cadence        rhea    floats (sun, hp)
> caeviews      cadence         rhea    floats (sun, hp)
> compile       cadence        rhea    floats (sun, hp)
> concept       cadence        rhea    floats (sun, hp)
> ged           cadence        rhea    floats (sun)
> packager      cadence         rhea    floats (sun, hp)
> verilog       cadence        rhea    floats (sun, hp)
> v2e           cadence        none    aphrodite (sun)
> 
> dracula       cadence         on node tomato cyclops medusa mothra (sun)
> 
> xvlsi         compass         none    abderus euterpe kephalos millennium
>                               poseidon ambiorix athena (sun)
> 
> vericheck     iss            hestia  tomato cyclops medusa mothra (sun)
> 
> energize      lucid          rhea    floats (sun)
> 
> hspice        meta-software  rhea    ambiorix ares boa frodo hera kephalos
>                              mercury merope narcissus pegasus
>                              pelorus phobos polyhymnia psyche thalia
> gsi           meta-software  rhea    floats (sun, hp)
> 
> hyperplot     pinebush        none    godzilla (sun)
> 
> capclc        silver-lisco   godzilla floats (sun)
> garout        silver-lisco   godzilla floats (sun)
> gplace        silver-lisco   godzilla floats (sun)
> maskout       silvar-lisco    godzilla floats (sun)
> pcomp         silvar-lisco    godzilla floats (sun)
> pgroute       silvar-lisco   godzilla floats (sun)
> redit         silvar-lisco   godzilla floats (sun)
> rdump         silvar-lisco    godzilla floats (sun)
> rload         silvar-lisco   godzilla floats (sun)
> slnet         silvar-lisco   godzilla floats (sun)
> 
> undertow      veritools      rhea    floats (sun)
> 
> edif22mif     zycad           none    nosferatu aphrodite (sun)
> linkmm        zycad           none    nosferatu aphrodite (sun)
> vxi           zycad          rhea    nosferatu aphrodite (sun)
> virsim        zycad          rhea    floats
> 
> 
> Vendor - License file Index:
> 
> Vendor: altium, tool: gerberview
> License binary: /n/auspex/s34/ecam
> License file: /n/auspex/s34/ecam/license.dat
> 
> Vendor: altium
> License binary: /a/pcad/license/bin.sun4
> License file: /a/pcad/license/pcadlic.dat
```

```
>
> Vendor: cadence
> License binary: /a/cadence/tools/bin
> License file: /a/cadence/share/license/license.55000dbe
>
> Vendor: cadence, tool: dracula
> License binary: /a/dracula4.1/tools/bin
> License file: /a/dracula4.1/share/license/license.55409301
>
> Vendor: lucid
> License binary: /s1/energize2.1/flexlm/bin           ???
> License file: /s1/energize2.1/flexlm/etc/license.dat    ???
>
> Vendor: silvar-lisco
> License binary: /a/silvar-lisco/license
> License file: /a/silvar-lisco/license/license.dat
>
> Vendor: sun, tool: fortran compiler
> License binary: /n/auspex/s34/fortran/license/bin4
> License file: /n/auspex/s34/fortran/license/bin4/license.dat
>
> Vendor: veritools
> License binary: /a/veritools/Lic.Mgr+typetool/license
> License file: /a/license/license.undertow
>
> Vendor: zycad
> License binary: /a/vxi/vxi_1.1/license
> License file: /a/license/license.vxi.1.1.combined
>
```

From: paulb (Paul Berry)

Sent: Wednesday, December 28, 1994 4:06 PM

To: 'lisar'; 'tbr'

Subject: Floating hols

Juli pointed out to me that I had misunderstood
the rules about floating holidays, and listed 12/26
as a date on which I was taking one of the two that
I had to spend.
I therefore revised my request so that it's for 12/27 and 12/30
(rather than 12/26-27).

In short, I hope to be out Friday after all.

/Paul

From:	woody (Jay Tomlinson)
Sent:	Wednesday, December 28, 1994 4:23 PM
To:	'lisar'
Cc:	'tbr'; 'mws'; 'billz'; 'dickson'; 'geert'
Subject:	BOM 198.0

Lisa,

I released BOM 198.0. It picks up everything that had been checked-in but not released.
Beware of the new euterpe_wrap.V that jeffm checked in. It gets a compile error. I did not
check in a new version since I do not know what was intended. Other than that, it ran my
local test to fab in all 5-cylinders.
I
ran out of the IBUF to get you a BOM faster. I will re-run from ROM locally.

Are there any dump files that needed attention? I saw some mail, but was unsure if they
were related to the fix that rich put into es.

Good Luck
Jay

From: lisar (Lisa Robinson)
Sent: Wednesday, December 28, 1994 4:32 PM
To: 'woody'
Cc: 'billz'; 'dickson'; 'geert'; 'mws'; 'tbr'
Subject: Re: BOM 198.0

Thanks. No I've no dumps as I think that the remaining problems may have been fixed
already. The test exlocktest fails (runs on terp) but I am unfamiliar with the test. The
zycad trace is in
/n/nosferatu/s2/euterpe/verilog/bsrc/res/281294.20247/results/exlocktest.d
po.

I'm trying to get to the bottom of a ikos problem running test1. I have BOM 197 so I
expect it to work. 3 of the cylinders fab but the other 2 just hang waiting for code from
the rom which doesn't respond. The timing is slightly from zycad or verilog and sc - phi
are phase offset by about 38 simticks.
I
just tried to reproduce it in verilog without any success. (skewed phi wrt sc).
I hope that it is a modelling problem ....

Lisa R.

From: Eric Murray [ericm@MicroUnity.com]

Sent: Wednesday, December 28, 1994 6:02 PM

To: 'Bill Zuravleff'

Cc: 'sysadmin@MicroUnity.com'; 'Mark Hofmann'; 'Tim B. Robinson'

Subject: Re: /s2/euterpe/verilog is Full!

Bill Zuravleff wrote:
>
> Help!
>   My euterpe workspace at /s2/euterpe/verilog/bsrc

it'd help if you'd give us the hostname too, though in
this case i already know it 'cause i get all the 'file system
full' messages.

> is full! Can't continue.
>
> In response to your next question, 95%+ of this data
> is auto-generated from the gards place and route steps.
> Yes, much of it can be removed, but not until I get to
> the final step.

even the verilog dump files?

if you can't remove anything, then we'll have to find
space on another disk.

the only other thing on that disk is a swapfile, and
that can't be touched without rebooting the machine.
and even then we'd get yelled at for not having enough swap on
the machine so you can pretty much guarantee that that
that swap file is not going anywhere.

--
    ericm   ericm@microunity.com

From:	tbr
Sent:	Wednesday, December 28, 1994 7:04 PM
To:	'Eric Murray'
Cc:	'Bill Zuravleff'; 'Mark Hofmann'; 'sysadmin@MicroUnity.com'
Subject:	Re: /s2/euterpe/verilog is Full!
Follow Up Flag: Follow up	
Flag Status:	Red

Eric Murray wrote (on Wed Dec 28):

Bill Zuravleff wrote:
>
> Help!
>   My euterpe workspace at /s2/euterpe/verilog/bsrc

it'd help if you'd give us the hostname too, though in
this case i already know it 'cause i get all the 'file system
full' messages.

OK, give the rest of us a clue. Where is it?

Tim

From: Eric Murray [ericm@angst]

Sent: Wednesday, December 28, 1994 7:09 PM

To: 'Tim B. Robinson'

Subject: Re: /s2/euterpe/verilog is Full!

Tim B. Robinson wrote:
>
>
> Eric Murray wrote (on Wed Dec 28):
>
>   Bill Zuravleff wrote:
>   >
>   > Help!
>   >   My euterpe workspace at /s2/euterpe/verilog/bsrc
>
>   it'd help if you'd give us the hostname too, though in
>   this case i already know it 'cause i get all the 'file system
>   full' messages.
>
> OK, give the rest of us a clue. Where is it?

ghidra.

--
   ericm   ericm@microunity.com

From: hopper (Mark Hofmann)

Sent: Thursday, December 29, 1994 11:03 AM

To: 'ken (Ken Hsieh)'

Cc: 'lisar (Lisa Robinson)'; 'tbr (Tim B. Robinson)'

Subject: zycad/vxi license woes

Hi Ken,

 I spoke with Zycad customer support. They say that with node-locked
licenses there is no way to combine license files. Therefore we need to
set up and maintain 2 separate copies of the license file, one for
Aphrodite and one for Psyche. We need to run a license server on each
machine. No floating license is available for VXI-Base.

Here is the latest key file:
```
#
#FLEXlm license file for hostid 55419dea:
#
SERVER <put.hostname.here> 55419dea 1701
DAEMON ZYCADD <put.correct.path.here>/zdaemon
FEATURE VXI-Base ZYCADD 2.020 29-dec-95 1 CBA9975F2D44DE8F01EC "" 55419dea


#
#FLEXlm license file for hostid 5540951e:
#
SERVER <put.hostname.here> 5540951e 1701
DAEMON ZYCADD <put.correct.path.here>/zdaemon
FEATURE VXI-Base ZYCADD 2.020 29-dec-95 1 5BA9679F2C9CCE9B3410 "" 5540951e
```

On the other hand, can we use these?

/a/license/license.vxi.1.1.5540951e:

```
SERVER rhea 55000dbe 5220
DAEMON stld /a/vxi/rel1.0d/license/stld1
FEATURE VXI-Base stld 1.100 31-dec-99 1 CB78B0B1D789FF5D5288 "SimTech" 5540951e
FEATURE VXI-XFault stld 1.100 31-dec-99 1 1B88D091D111C28E0F9C "SimTech" 5540951e
```

/a/license/license.vxi.1.1.55419dea:

```
SERVER rhea 55000dbe 5212
DAEMON stld /a/vxi/rel1.0d/license/stld2
FEATURE VXI-Base stld 1.100 31-dec-99 1 3B1880B19C630F075194 "SimTech" 55419dea
FEATURE VXI-XFault stld 1.100 31-dec-99 1 5BE840F17001526AE0A2 "SimTech" 55419dea
```

Ken, these already exist and should work. If you can get these running,
then perhaps Lisa can point to both /a/license/license.vxi.1.1.55419dea and
/a/license/license.vxi.1.1.5540951e

-thanks,
hopper

From: hopper (Mark Hofmann)

Sent: Thursday, December 29, 1994 11:30 AM

To: 'Lisa Robinson'

Cc: 'ken (Ken Hsieh)'; 'tbr (Tim B. Robinson)'

Subject: Re: vxi

Lisa Robinson writes:
  I am running on aphrodite.

  Lisa R.

  VXI 1.1   Thu Dec 29 16:32:45 1994
    * Copyright Simulation Technologies Corporation 1992. *
    *   All Rights Reserved.   Licensed Software.   *
  Error [-8]; feature "VXI-Base"
  encryption code in license file is inconsistent
  gmake[1]: *** [.xp_dir/c_euterpe_wrap.edif2] Error 1
  gmake[1]: Leaving directory `/s3/euterpe/verilog/bsrc'
  gmake: *** [czycad] Error 1

I have reverted to 5.0. Please try again.

-hopper

From: lisar (Lisa Robinson)

Sent: Thursday, December 29, 1994 12:44 PM

To: 'hopper'; 'tbr'; 'ken'

Subject: VXI license

VXI 1.1   Thu Dec 29 10:40:30 1994
 * Copyright Simulation Technologies Corporation 1992. *
 *   All Rights Reserved.   Licensed Software.   *
Error [-8]; feature "VXI-Base"
encryption code in license file is inconsistent
gmake[1]: *** [.xp_dir/c_euterpe_wrap.edif2] Error 1
gmake[1]: Leaving directory `/s3/euterpe/verilog/bsrc'
gmake: *** [czycad] Error 1

Which file should the Makefile.defs be pointing at?

Lisa R.

From: ken (Ken Hsieh)

Sent: Thursday, December 29, 1994 1:15 PM

To: 'Lisa Robinson'

Cc: 'tbr (Tim B. Robinson)'; 'hopper (Mark Hofmann)'; 'ken (Ken Hsieh)'

Subject: Re: VXI license

Lisa,

I "think" you should use /a/license/license.vxi.1.1.combined.6.0.

Ken

```
>
>
> VXI 1.1   Thu Dec 29 10:40:30 1994
>   * Copyright Simulation Technologies Corporation 1992. *
>   *    All Rights Reserved.    Licensed Software.    *
> Error [-8]; feature "VXI-Base"
> encryption code in license file is inconsistent
> gmake[1]: *** [.xp_dir/c_euterpe_wrap.edif2] Error 1
> gmake[1]: Leaving directory `/s3/euterpe/verilog/bsrc'
> gmake: *** [czycad] Error 1
>
> Which file should the Makefile.defs be pointing at?
>
> Lisa R.
>
```

BP,

   OK! I have a 6t cell with NO m2 or m3 on it just as Mousse wanted.
It
also has the bit lines, vss, and vdd lines running vertically. The word line is in poly
running horizontally. There are actually 2 poly word lines on the cell which would have
to be merged outside the array. It looks very nice (my opinion, of course). Please look
at it, inspect it, or critique it.
Right
now, it's the best that I can come up with. By the way, the dimensions are
12 by 10.2 (122.4 u2). Not quite the 100 u2 that you wanted but I think you'll be happy
with this. Let me know what you think tomorrow.

search path: ~efelias/csm/euterpe

cell name: csm6tm1 (single cell) - no m2 or m3
            csm6tm18x8 (arrayed 8x8)

            csm6tc (single cell but with m2)
            csm6tm28x8 (arrayed 8x8)

            csm6tcell (single cell with m2 and m3)
            csm6tm38x8 (arrayed 8x8)

Eldred

--

From: lisar (Lisa Robinson)

Sent: Thursday, December 29, 1994 1:27 PM

To: 'ken (Ken Hsieh)'

Cc: 'hopper (Mark Hofmann)'; 'tbr (Tim B. Robinson)'

Subject: Re: VXI license

Ken Hsieh wrote (on Thu Dec 29):

Lisa,

I "think" you should use /a/license/license.vxi.1.1.combined.6.0.

Ken

Well I am pointing at:

1 lrwxrwxrwx 1 ken   28 Dec 27 10:50 /a/license/license.vxi.1.1.combined -> license.vxi.1.1.combined.6.0

Lisa R.

```
>
>
> VXI 1.1   Thu Dec 29 10:40:30 1994
>  * Copyright Simulation Technologies Corporation 1992. *
>  *    All Rights Reserved.    Licensed Software.    *
> Error [-8]; feature "VXI-Base"
> encryption code in license file is inconsistent
> gmake[1]: *** [.xp_dir/c_euterpe_wrap.edif2] Error 1
> gmake[1]: Leaving directory `/s3/euterpe/verilog/bsrc'
> gmake: *** [czycad] Error 1
>
> Which file should the Makefile.defs be pointing at?
>
> Lisa R.
>
```

From: tbr

Sent: Thursday, December 29, 1994 2:20 PM

To: 'lisar'

Cc: 'craig'; 'dbulfer'

Subject: architecture manual

Follow Up Flag: Follow up

Flag Status: Red

Please print a copy of the latest release of the Terpsichore
Architecture Document for David Bulfer.

Thanks
Tim

From: tbr

Sent: Thursday, December 29, 1994 4:01 PM

To: 'lisar'

Subject: IKOS compile

Follow Up Flag: Follow up

Flag Status: Red

I just tried a new compile in my bsrc area and it failed:

s_ieee=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/lib/vhdl/sun_sparc/ieee
PATH=/n/auspex/s15/tbr/euterpe/tools/vendor/ikos/voyager_2.0/bin/sun_sparc:$PATH /n/auspex/s15/tbr/euterpe/tools/vendc
i_euterpe_wrap.vhdl

```
                poko          in: std_logic;
        -------------------------------^
E L8/C9:      unexpected symbol "'in'" encountered
REPAIR:   'in'@L8/C9 was deleted

                rdata         out: std_logic_vector (63 downto 0);
        -------------------------------^
E L9/C12:     unexpected symbol "'out'" encountered
REPAIR:   'out'@L9/C12 was deleted

                sdclock0_abm   out: std_logic;
        -------------------------------^
E L10/C17:    unexpected symbol "'out'" encountered
REPAIR:   'out'@L10/C17 was deleted

                sdc_abm        out: std_logic_vector (4 downto 0);
        -------------------------------^
E L11/C14:    unexpected symbol "'out'" encountered
REPAIR:   'out'@L11/C14 was deleted

                sda_abm        out: std_logic_vector (12 downto 0);
        -------------------------------^
E L12/C13:    unexpected symbol "'out'" encountered
REPAIR:   'out'@L12/C13 was deleted

                sdd_abm        inout: std_logic_vectore (31 downto 0)
        -------------------------------^
E L13/C12:    unexpected symbol "'inout'" encountered
REPAIR:   'inout'@L13/C12 was deleted
%VHDL-I-SyntaxError, design unit not created due to syntax error
```

any idea what's going on.

Tim

From:	ong (Warren R. Ong)
Sent:	Thursday, December 29, 1994 4:23 PM
To:	'vo (Tom Vo)'; 'bpw (B. P. Wong)'; 'stick (Bruce Bateman)'; 'geert (Geert Rosseel)'; 'tom (Thomas Laidig)'; 'vanthof (Dave Van't Hof)'; 'wampler (Kurt Wampler)'; 'tbr (Tim B. Robinson)'
Cc:	'ong (Warren R. Ong)'
Subject:	Euterpe Power Buss Concerns

Hi,

Extracted metals forming the power buss structure of euterpe were visually inspected. The areas that were closely examined were the areas that would load on to Compass. Some areas were found to have problems, other areas could be improved. A list of the areas are listed below. I have plots in my office, but they do not show much detail.

(I) IMPORTANT FIXES

(a) Ends of Clock Spars
  The verticle M3 around the power pillars were designed to drive
  the atoms half way to the next power pillar (5 rows of atoms).
  The top and bottom ends of the array may have 9 rows of atoms
  from the last power pillar to the edge of the sofa array. M3
  needs to be supported by the hemming cell and/or power rings at
  the edges. (There are edges at the pads and at custom block
  interfaces).

(b) Power to GTLB
  GTLB needs a stronger power connection to its I/O edge. Can
  power pillars be added internally to GTLB?

(c) I & D Cache
  There is an I*R drop to the Cache/SOFA interface that is
  double of the SOFA's I*R drop. The typical I*R drop in the SOFA
  (assuming rcd6, 80% isrc utilization) is 29.7mV. The Cache will
  have about 64.3mV of drop at its interface. Power is fed to the
  Cache from the SOFA row that is 70% the length of a whole row.

(II) NORMAL FIXES

(a) "ledsegdrv" add more M4 -> M2 connections from power ring
  to hemming cells. Do not touch any of the pad layouts.

(b) "iobyte" add more M4 connections from power ring to hemming cell

(c) "clio" add M4 power ring to hemming connections cell

(d) cmos_regfile: missing/broken M4 @ x179105y5487 wrt euterpe origin
               : join M4 power straps to hemming cells in the middle

(III) MINOR FIXES
(a) horizontal M2 gap ~x118800y189600
(b) "cache" connect power metals to hemming cells
(c) "cache" M2 gap ~x187200y119000 from euterpe's origin
(d) "ctag" connect power metals to hemming cells
(e) "cerberus" fill in hemming cells where ever possible

(IV) QUESTIONABLE
(a) Should we add power pillars to the hemming cells between ctags?
(b) Should we add power pillars to the hemming cells between plls?
(c) Can we remove the single row of atom below cmos_regfile if it is
  unused?
(d) Is there enough power to to belly buttons on the top edge?

Warren.

From:	tbr
Sent:	Thursday, December 29, 1994 6:50 PM
To:	'lisar'
Subject:	euterpe_wrap
Follow Up Flag:	Follow up
Flag Status:	Red

I had not done the update. vlit compiled it apparantly without complaining! However, it's definitiely missing the declarations.

Tim

From: geert (Geert Rosseel)

Sent: Thursday, December 29, 1994 7:08 PM

To: 'billz'; 'brianl'; 'dickson'; 'geert'; 'hopper'; 'mws'; 'tbr'; 'vo'; 'woody'

Subject: Euterpe timing analysis

Hi,

I build Euterpe - BOM 197.0 and ran a timing analysis. Here are the bad paths.

****

This first set is all related to the same thing. It is a fanout of nb
to 3 different blocks. The wire estimate is really long. I am
not sure how the nof data is calculated for wires with multiple
fan-out

****
dr to nb
****

Warning! Cycle time exceeded by 1.88ps using cycle time of 926.00 for Iteration 1   HARD ERROR 1
    Path After Optimization using cycle time of 926.00:   dr/drout/muxff7_16prblo/u9   (xbmuxffb7dh24s 24S) Oport:
q_and0ph IntDel: 89.60 net: DRprb_N<9> swg: dh   delay: 279.59ps (force) RC delay: 157.62ps   lds: 1 pcap: 20.73ff
cap: 595.26ff (ext) m2len: 0.00 m3len: 5223.00 m4len: 0   nb/mux4_16_prba/u9   (xbmux4dh16s 16S)   Iport:
D3_AND0PH   Oport: q_ad0ph IntDel: 83.80 net: nb/prb<9>   swg: dh delay: 106.50ps (force) RC delay:
23.13ps   lds: 3 pcap: 36.75ff cap: 241.75ff (ext) m2len: 0.00 m3len: 1230.00 m4len: 574.00
    nb/muxenff2_5oq/u4/u0 (xbmuxen2dh16s 16S)   Iport: D1_AD0PH Oport: q_ad0ph IntDel: 72.60 net:
nb/muxenff2_5oq/u4/m   swg: dh delay: 8.49ps (force) RC delay: 0.17ps   lds: 1 pcap: 7.52ff cap: 21.32ff (ext)
m2len: 0.00 m3len: 50.00 m4len: 88.00
    nb/muxenff2_5oq/u4/u1 (xbffdh6s 6S)   Iport: D0_ADMPH IntDel: 287.30
    Time through Path: 927.88

****
nb to hc0
****

Warning! Cycle time exceeded by 298.77ps using cycle time of 926.00 for Iteration 1   HARD ERROR 5
    Path After Optimization using cycle time of 926.00:
    nb/muxenff4_32pbb/u31/u1   (xbffbdh24s 24S)   Oport: q_ad0ph IntDel: 89.20 net: NBpbb<31> swg: dh
delay: 946.97ps (force) RC delay: 665.56ps   lds: 8 pcap: 70.01ff cap: 1232.05ff (ext) m2len: 0.00 m3len: 10564.00
m4len: 0.00
    hc0/u100/u31 (xbffdf32s 32S)   Iport: D0_ADMPH IntDel: 188.60
    Time through Path: 1224.77

****
nb to hc1
****

Warning! Cycle time exceeded by 295.57ps using cycle time of 926.00 for Iteration 1   HARD ERROR 9
    Path After Optimization using cycle time of 926.00:

nb/muxenff4_32pbb/u31/u1   (xbffbdh24s 24S)   Oport: q_ad0ph IntDel: 89.20 net: NBpbb<31> swg: dh
delay: 946.97ps (force) RC delay: 665.56ps   lds: 8 pcap: 70.01ff cap: 1232.05ff (ext) m2len: 0.00 m3len: 10564.00
m4len: 0.00
    hc1/u101/u10 (xbffdf24s 24S)   Iport: D0_ADMPH IntDel: 185.40
    Time through Path: 1221.57

****
nb to gt
****

Warning! Cycle time exceeded by 356.87ps using cycle time of 926.00 for Iteration 1   HARD ERROR 19
    Path After Optimization using cycle time of 926.00:
    nb/muxenff4_32pbb/u31/u1   (xbffbdh24s 24S)   Oport: q_and0ph IntDel: 89.20 net: NBpbb_N<31>
swg: dh delay: 946.97ps (force) RC delay: 665.56ps   lds: 8 pcap: 70.01ff cap: 1232.05ff (ext) m2len: 0.00 m3len:
10564.0 m4len: 0.00
    gt/UgtSnake/Upbbo/u31 (xbmuxff2df32s 32S)   Iport: D0_AND0PH   IntDel: 246.70
    Time through Path: 1282.87

****

****
nb to dr
****

Warning! Cycle time exceeded by 11.97ps using cycle time of 926.00 for Iteration 1   HARD ERROR 363
    Path After Optimization using cycle time of 926.00:
    nb/nbprbarb/Ug0/u0   (xborffb8df32s 32S)   Oport: Q_AD0PF IntDel: 87.80 net: NBdrprgrant_N   swg: df delay:
360.54ps (force) RC del
ay: 129.33ps lds: 7 pcap: 48.88ff cap: 549.16ff (ext) m2len: 0.00 m3len: 4548.00 m4len: 0.00
    dr/drout/drprbcsm/Ufull_0_10/u0 (xbor7df32s 32S)   Iport: D3_A0PF Oport: Q_AND0PF IntDel: 220.90 net:
dr/drout/drprbcsm/full_N_0_10
    swg: df delay: 25.74ps (force) RC delay: 0.78ps   lds: 4 pcap: 22.74ff cap: 49.44ff (ext) m2len: 0.00 m3len:
193.00 m4len: 74.00
    dr/drout/drprbcsm/Uprcount_0/u0 (xborff7df6s 6S)   Iport: D6_A0PF IntDel: 243.00
    Time through Path: 937.97

****
nb to uu
****

Warning! Cycle time exceeded by 285.60ps using cycle time of 926.00 for Iteration 1   HARD ERROR 366
    Path After Optimization using cycle time of 926.00:
    nb/nbctrl/Udreforreturn/u0   (xborffb3dh24s 24S)   Oport: q_ad0ph IntDel: 89.60 net: nb/dreforreturn_N swg: dh
delay: 12.43ps (force)
    RC delay: 0.50ps   lds: 2 pcap: 16.52ff cap: 57.82ff (ext) m2len: 129.00 m3len: 26.00 m4len: 0.00
    nb/bufNBwed/u0 (xbbufdf32s 32S)   Iport: D0_ANDMPH   Oport: Q_AD0PF IntDel: 107.60 net: nbWeDX1
swg: df delay: 708.97ps (force
)   RC delay: 363.79ps   lds: 13 pcap: 64.46ff cap: 915.09ff (ext) m2len: 0.00 m3len: 7733.00 m4len: 0.00
    uu/UnbOutBsy/u0 (xbmuxff2df8s 8S)   Iport: SEL_A0PEH<1>   IntDel: 293.00
    Time through Path: 1211.60

****
cc to nb
****

Warning! Cycle time exceeded by 34.15ps using cycle time of 926.00 for Iteration 1   HARD ERROR 449
    Path After Optimization using cycle time of 926.00:
    cc/muxff4_16_nbcout/u4 (xbmuxffb4df32s 32S)   Oport: Q_AD0PF IntDel: 89.50 net: CCnbcout<4>   swg: df

delay: 428.08ps (force) RC del

ay: 167.80ps   lds: 40 pcap: 252.00ff cap: 708.28ff (ext) m2len: 0.00 m3len: 4148.00 m4len: 0.00
    nb/fqueue/nbfqslice0/Un0_5/u0 (xbor3df32s 32S)   Iport: D2_A0PF Oport: Q_AND0PF IntDel: 179.80 net:
nb/fqueue/nbfqslice0/n0_N_5
    swg: df delay: 10.87ps (force) RC delay: 0.19ps   lds: 1 pcap: 6.04ff   cap: 21.74ff (ext) m2len: 0.00 m3len: 13.00
m4len: 144.00
    nb/fqueue/nbfqslice0/Un0/u0   (xborffb8df12s 12S)   Iport: D5_A0PF IntDel: 251.90
        Time through Path: 960.15

 Warning! Cycle time exceeded by 33.05ps using cycle time of 926.00 for Iteration 1   HARD ERROR 591
    Path After Optimization using cycle time of 926.00:
      cc/muxff3_16_aouthi/u14 (xbmuxffb3df32s 32S)   Oport: Q_AD0PF IntDel: 87.80   net: CCnbaout<46>   swg: df
delay: 385.50ps (force) RC del

ay: 121.06ps   lds: 23 pcap: 269.08ff cap: 630.10ff (ext) m2len: 0.00 m3len: 3282.00 m4len: 0.00
    nb/nbctrl/Upushpqhc0m1_4/u0   (xbor11df32s 32S)   Iport: D9_A0PF Oport: Q_AND0PF IntDel: 222.30 net:
nb/nbctrl/pushpqhc0m1_N_4 swg: d
f   delay: 19.65ps (force) RC delay: 0.38ps   lds: 1 pcap: 6.06ff   cap: 38.76ff (ext) m2len: 71.00 m3len: 114.00
m4len: 0.00
    nb/nbctrl/Upushpqhc0m1/u0   (xborff8dh6s 6S)   Iport: D4_A0PF IntDel: 243.80
        Time through Path: 959.05

 Warning! Cycle time exceeded by 245.36ps using cycle time of 926.00 for Iteration 1   HARD ERROR 611
    Path After Optimization using cycle time of 926.00:
      cc/ccstart/Unbgo/u0   (xborffb7df32s 32S)   Oport: Q_AD0PF IntDel: 89.50   net: CCnbgo_N swg: df delay:
578.79ps (force) RC delay: 240.
31ps   lds: 44 pcap: 449.48ff cap: 927.10ff (ext) m2len: 0.00 m3len: 4342.00 m4len: 0.00
    nb/fqcount/Ucout_2_6/u0 (xbor4df32s 32S) Iport: D3_A0PF Oport: Q_AND0PF IntDel: 184.10 net:
nb/fqcount/cout_N_2_6   swg: df delay:
41.67ps (force)   RC delay: 2.49ps   lds: 2 pcap: 14.29ff cap: 75.59ff (ext) m2len: 0.00 m3len: 207.00 m4len:
406.00
    nb/fqcount/Ucouta_2/u0 (xborff13df12s 12S)   Iport: D6_A0PF IntDel: 277.30
        Time through Path: 1171.36

****
in gt
****

    Path After Optimization using cycle time of 926.00:
      gt/UgtSnake/Upbbo/u16 (xbmuxffb2df32s 32S)   Oport: Q_AD0PF IntDel: 86.50   net: GIpbb<16> swg: df delay:
408.61ps (force) RC delay: 145.
28ps   lds: 5 pcap: 44.20ff cap: 579.46ff (ext) m2len: 0.00 m3len: 4866.00 m4len: 0.00
    gt/UgtSnake/UspMtchErly/Uresetrdy_2/u0 (xbor17df32s 32S)   Iport: D0_A0PF Oport: Q_AND0PF IntDel: 244.20
net: gt/UgtSnake/UspMtchErly/r
esetrdy_N_2   swg: df delay: 6.74ps (force) RC delay: 0.08ps lds: 1 pcap: 4.92ff   cap: 14.42ff (ext) m2len: 0.00
m3len: 13.00 m4len: 82.00
    gt/UgtSnake/UspMtchErly/Uresetrdy/u0   (xborff3df2s 2S)   Iport: D2_A0PF IntDel: 266.30
        Time through Path: 1012.35

 Warning! Cycle time exceeded by 12.20ps using cycle time of 926.00 for Iteration 1   HARD ERROR 720
    Path After Optimization using cycle time of 926.00:
      gt/UgtSnake/Upbbo/u27 (xbmuxffb2df32s 32S)   Oport: Q_AD0PF IntDel: 90.00   net: GIpbb<27> swg: df delay:
489.00ps (force) RC delay: 235.
67ps   lds: 7 pcap: 61.55ff cap: 739.81ff (ext) m2len: 0.00 m3len: 6166.00 m4len: 0.00
    gt/UgtSnake/Ushift43/u3 (xbmuxff6dh3s 3S)   Iport: D4_AD0PH IntDel: 359.20
        Time through Path: 938.20

****

gt to at
****

Warning! Cycle time exceeded by 2.55ps using cycle time of 926.00 for Iteration 1   HARD ERROR 749
    Path After Optimization using cycle time of 926.00:
        gt/UsaoutXorR10/u4   (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 91.30 net: GIsaOutR10<20>   swg: df delay:
144.08ps (force) RC del
ay: 42.23ps   lds: 5 pcap: 34.51ff cap: 316.11ff (ext) m2len: 0.00 m3len: 2560.00 m4len: 0.00
        at/UatPaSel/UpaSel10/u0 (xbmux3df16s 16S)   Iport: D1_AD0PH Oport: Q_AND0PF IntDel: 211.10 net:
at/paR10_N<10>   swg: df delay: 231.67p
s (force)   RC delay: 22.90ps   lds: 2 pcap: 14.81ff cap: 218.71ff (ext) m2len: 0.00 m3len: 1480.00 m4len: 559.00
        at/Upa1509EqfefR11/u0 (xborff7df12s 12S)   Iport: D1_A0PF IntDel: 250.40
        Time through Path: 928.55

****
at to ctiod
****

Warning! Cycle time exceeded by 156.31ps using cycle time of 926.00 for Iteration 1   HARD ERROR 755
    Path After Optimization using cycle time of 926.00:
        at/UvldStrR15/u0   (xbffbdh24s 24S)   Oport: q_ad0ph IntDel: 89.60 net: ATvldStrR15   swg: dh delay:
622.30ps (force) RC del
ay: 423.89ps   lds: 3 pcap: 23.78ff cap: 972.97ff (ext) m2len: 0.00 m3len: 8629.00 m4len: 0.00
        ctiod/dor2_d0/u0   (xbmux2dh16s 16S)   Iport: SEL_A0PEH<1>   Oport: q_and0ph IntDel: 111.40 net:
ctiod/d0_N swg: dh delay: 5.01ps
(force) RC delay: 0.02ps   lds: 1 pcap: 7.80ff   cap: 13.00ff (ext) m2len: 16.00 m3len: 4.00 m4len: 0.00
        ctiod/muxff2_32dinlo/u0 (xbmuxff2df4s forced 4S)   Iport: D1_AND0PH   IntDel: 254.00
        Time through Path: 1082.31

******
at to uu
******

Warning! Cycle time exceeded by 102.83ps using cycle time of 926.00 for Iteration 1   HARD ERROR 757
    Path After Optimization using cycle time of 926.00:
        at/UvldStrR15/u0   (xbffbdh24s 24S)   Oport: q_ad0ph IntDel: 89.20 net: ATvldStrR15   swg: dh delay:
645.63ps (force) RC del
ay: 423.89ps   lds: 3 pcap: 23.78ff cap: 972.97ff (ext) m2len: 0.00 m3len: 8629.00 m4len: 0.00
        uu/UvldTdWrtR16/u0   (xbmuxff2dh2s 2S)   Iport: D0_AD0PH IntDel: 294.00
        Time through Path: 1028.83

****

These are also all related

****
uu to ife
****

Warning! Cycle time exceeded by 828.29ps using cycle time of 926.00 for Iteration 1   HARD ERROR 762
    Path After Optimization using cycle time of 926.00:
        uu/Urst9CUS/u0 (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 90.00 net: UUrstUS swg: df delay: 1448.09ps
(force)   RC delay: 953.
15ps   lds: 13 pcap: 99.73ff cap: 1479.68ff(ext) m2len: 0.00 m3len: 12545.00 m4len: 0.00
        ife/UrstUS0C/u0 (xbffdf4s 4S)   Iport: D0_ADMPH IntDel: 216.20
        Time through Path: 1754.29

```
*******
uu to iq
*******
```

Warning! Cycle time exceeded by 789.89ps using cycle time of 926.00 for Iteration 1   HARD ERROR 763
    Path After Optimization using cycle time of 926.00:
        uu/Urst9CUS/u0 (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 90.00   net: UUrstUS   swg: df delay: 1448.09ps
(force)   RC delay: 953.
15ps   lds: 13 pcap: 99.73ff   cap: 1479.68ff (ext) m2len: 0.00 m3len: 12545.00 m4len: 0.00
        iq/Urst0C/u0   (xbffdf12s 12S)   Iport: D0_ADMPH IntDel: 177.80
        Time through Path: 1715.89

```
*******
uu to at
*******
```

Warning! Cycle time exceeded by 786.89ps using cycle time of 926.00 for Iteration 1   HARD ERROR 764
    Path After Optimization using cycle time of 926.00:
        uu/Urst9CUS/u0 (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 90.00   net: UUrstUS   swg: df delay: 1448.09ps
(force)   RC delay: 953.
15ps   lds: 13 pcap: 99.73ff   cap: 1479.68ff (ext) m2len: 0.00 m3len: 12545.00 m4len: 0.00
        at/Ureset/u0   (xbffdf16s 16S)   Iport: D0_ADMPH IntDel: 174.80
        Time through Path: 1712.89

```
*******
uu to lt
*******
```

Warning! Cycle time exceeded by 899.39ps using cycle time of 926.00 for Iteration 1   HARD ERROR 765
    Path After Optimization using cycle time of 926.00:
        uu/Urst9CUS/u0 (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 90.00   net: UUrstUS   swg: df delay: 1448.09ps
(force)   RC delay: 953.
15ps   lds: 13 pcap: 99.73ff   cap: 1479.68ff (ext) m2len: 0.00 m3len: 12545.00 m4len: 0.00
        lt/Ureset/u0   (xbffdh6s 6S)   Iport: D0_ADMPH IntDel: 287.30
        Time through Path: 1825.39

```
*******
uu to gt
*******
```

Warning! Cycle time exceeded by 899.39ps using cycle time of 926.00 for Iteration 1   HARD ERROR 766
    Path After Optimization using cycle time of 926.00:
        uu/Urst9CUS/u0 (xbffbdf32s 32S)   Oport: Q_AD0PF IntDel: 90.00   net: UUrstUS   swg: df delay: 1448.09ps
(force)   RC delay: 953.
15ps   lds: 13 pcap: 99.73ff   cap: 1479.68ff(ext) m2len: 0.00 m3len: 12545.00 m4len: 0.00
        gt/Ureset/u0   (xbffdh2s 2S)   Iport: D0_ADMPH IntDel: 287.30
        Time through Path: 1825.39

```
*****************************************************************************************************

*******
in uu
*****
```

lots of errors

```
*******
uu to at
```

****

Warning! Cycle time exceeded by 287.54ps using cycle time of 926.00 for Iteration 1   HARD ERROR 1759
    Path After Optimization using cycle time of 926.00:
        uu/UvldNoXcR11/u0   (xborffb3df32s 32S)   Oport: Q_AD0PF IntDel: 86.50   net: UUvldNoXcR11_N   swg: df
delay: 579.01ps (force) RC del
ay: 236.31ps   lds: 13 pcap: 109.49ff cap: 757.94ff (ext) m2len: 0.00 m3len: 5895.00 m4len: 0.00
        at/Uatpadcd/UvldNonNbSt_2/u0   (xbor13df32s 32S)   Iport: D5_A0PF Oport: Q_AND0PF IntDel: 253.50 net:
at/Uatpadcd/vldNonNbSt_N_2 swg: d
f   delay: 17.23ps (force) RC delay: 0.19ps   lds: 1 pcap: 5.97ff   cap: 32.47ff (ext) m2len: 77.00 m3len: 34.00
m4len: 0.00
        at/Uatpadcd/UvldNonNbSt/u0   (xborff7dh3s 3S)   Iport: D2_A0PF IntDel: 277.30
        Time through Path: 1213.54

****
These are also related

****
uu to cdio
****

Warning! Cycle time exceeded by 262.73ps using cycle time of 926.00 for Iteration 1   HARD ERROR 1920
    Path After Optimization using cycle time of 926.00:
        uu/UetaBffrdUT/u0   (xbffbdh24s 24S)   Oport: q_ad0ph IntDel: 89.20   net: UUetaUT<0> swg: dh delay:
892.53ps (force) RC delay: 621.
04ps   lds: 9 pcap: 63.96ff cap: 1188.93ff (ext) m2len: 0.00 m3len: 10227.00 m4len: 0.00
        cdio/UwrCtlAc/u0   (xbhrdh3s 3S)   Iport: D0_AD0PH IntDel: 207.00
        Time through Path: 1188.73

****
uu to mc
****

Warning! Cycle time exceeded by 271.55ps using cycle time of 926.00 for Iteration 1   HARD ERROR 1926
    Path After Optimization using cycle time of 926.00:
        uu/UetaBffrdUT/u0   (xbffbdh24s 24S)   Oport: q_and0ph IntDel: 89.20   net: UUetaUT_N<0>   swg: dh delay:
891.25ps (force) RC del
ay: 619.99ps   lds: 9 pcap: 63.96ff cap: 1187.94ff (ext) m2len: 0.00 m3len: 10218.00 m4len: 0.00
        mc/u206/u0   (xbhrdh2s 2S)   Iport: D0_AND0PH   IntDel: 217.10
        Time through Path: 1197.55

****

There is also a problem with these signals from uu :

Warning! Cycle time exceeded by 1386.32ps using cycle time of 926.00 for Iteration 1 HARD ERROR 1993
    Path After Optimization using cycle time of 926.00:
        uu/UtauOutUU/u0 (xbffedh24s 24S)   Oport: q_ad1ph IntDel: 127.90 net: UUtauUU   swg: dh delay: 1967.32ps
(force)   RC delay: 1628
.82ps   lds: 26 pcap: 707.06ff cap: 2168.74ff (ext) m2len: 0.00 m3len: 13288.00 m4len: 0.00
        hz/hzmatch_hz/hr_clmatch/u0   (xbhrdh2s 2S)   Iport: TAU_AD1PH   IntDel: 217.10
        Time through Path: 2312.32

Warning! Cycle time exceeded by 485.79ps using cycle time of 926.00 for Iteration 1   HARD ERROR 2032
    Path After Optimization using cycle time of 926.00:
        uu/UpsiUP/u0   (xbmuxffb2df32s 32S)   Oport: Q_AND0PF IntDel: 87.80   net: UUpsiUP_N<0>   swg: df delay:

780.56ps (force) RC delay: 385.

14ps lds: 11 pcap: 88.48ff cap: 949.12ff (ext) m2len: 0.00 m3len: 7824.00 m4len: 0.00
    uu/prblmup/UnbLdrOkPreemRqstUQ_0/u0   (xbor8df32s 32S)   Iport: D7_A0PF Oport: Q_AND0PF IntDel:
229.10 net: uu/prblmup/nbLdrOkPreemRq
stUQ_N_0   swg: df delay: 39.93ps (force) RC delay: 0.87ps   lds: 5 pcap: 34.74ff cap: 72.44ff (ext) m2len: 88.00
m3len: 113.00 m4len
: 0.00
    uu/prblmup/UbFtchOkPreemRqstUQ/u0   (xborffl3df16s 16S)   Iport: D3_A0PF IntDel: 274.40
    Time through Path: 1411.79

****
iq to uu to rgxmit
****

Warning! Cycle time exceeded by 137.78ps using cycle time of 926.00 for Iteration 1   HARD ERROR 2160
    Path After Optimization using cycle time of 926.00:
    iq/UinstLQS/u7 (xbmuxffb8dh24s 24S) Oport: q_ad0ph IntDel: 89.60 net: IQinstQS<7>   swg: dh delay:
474.45ps (force) RC delay: 305.
68ps lds: 1 pcap: 21.09ff cap: 826.52ff (ext) m2len: 0.00 m3len: 7322.00 m4len: 0.00
    uu/UinstUQ/u7 (xbmux3dh16s 16S)   Iport: D2_AD0PH Oport: q_and0ph IntDel: 74.00   net: UUinstUQ_N<7>
swg: dh delay: 208.03ps (force
)   RC delay: 66.11ps   lds: 2 pcap: 19.52ff cap: 387.47ff (ext) m2len: 0.00 m3len: 3345.00 m4len: 0.00
    rgxmit/Urc51RL/u0   (xbffdh24s 24S)   Iport: D0_ANDMPH   IntDel: 217.70
    Time through Path: 1063.78

From: lisar (Lisa Robinson)

Sent: Thursday, December 29, 1994 7:20 PM

To: 'hopper'

Cc: 'ken'; 'tbr'

Subject: Re: vxi

I am running on aphrodite.

Lisa R.

```
VXI 1.1   Thu Dec 29 16:32:45 1994
  * Copyright Simulation Technologies Corporation 1992. *
  *    All Rights Reserved.    Licensed Software.    *
Error [-8]; feature "VXI-Base"
encryption code in license file is inconsistent
gmake[1]: *** [.xp_dir/c_euterpe_wrap.edif2] Error 1
gmake[1]: Leaving directory `/s3/euterpe/verilog/bsrc'
gmake: *** [czycad] Error 1
^C
```

From: tbr

Sent: Thursday, December 29, 1994 7:26 PM

To: 'lisar'

Subject: pass.run

Follow Up Flag: Follow up

Flag Status: Red

I tried it in my area:

```
40    sh  cp ../../verify/toplevel/./test1_0.slr .
41    sh  cp ../../verify/toplevel/./test1_0.sig .
42    stimxl -c 0 eu.bs
stimxl: Error (TvshCmd::NoSuchFile): Couldn't open stimulus file /N/auspex/root/s15/tbr/euterpe/verilog/bsrc/eu.bs
```

I copied that over, then it complained about the .wav file and I
copied that one too. Where should they be comming from?

Tim

Geert Rosseel wrote ....
>
>
>Hi,
>
>I build Euterpe - BOM 197.0 and ran a timing analysis. Here are the bad
paths.
>
>***
>**
****
>
>This first set is all related to the same thing. It is a fanout of nb
>to 3 different blocks. The wire estimate is really long. I am not sure
>how the nof data is calculated for wires with multiple fan-out
>

>
>Warning! Cycle time exceeded by 298.77ps using cycle time of 926.00
>for
Iteration 1   HARD ERROR 5
>   Path After Optimization using cycle time of 926.00:
>   nb/muxenff4_32pbb/u31/u1   (xbffbdh24s 24S)   Oport:
q_ad0ph IntDel: 89.20   net: NBpbb<31> swg: dh   delay: 946.97ps
(force) RC delay: 665.56ps   lds: 8 pcap: 70.01ff   cap: 1232.05ff
(ext) m2len: 0.00 m3len: 10564.00 m4le>n: 0.00
>   hc0/u100/u31   (xbffdf32s 32S)   Iport: D0_ADMPH IntDel:
188.60
>   Time through Path: 1224.77
>
>

This wire length looks real . NBpbb goes to hc0,1,gt and dr .
Just for going to the new dr placement , we picked up some 3mm in length .

tvo

From: lisar (Lisa Robinson)
Sent: Thursday, December 29, 1994 7:31 PM
To: 'tbr'
Subject: Re: pass.run

do this ..

in euterpe

ln -s /n/nosferatu/s2/euterpe/verify

Lisa R.

From:	tbr
Sent:	Thursday, December 29, 1994 7:35 PM
To:	'lisar (Lisa Robinson)'
Subject:	Re: pass.run
Follow Up Flag:	Follow up
Flag Status:	Red

Lisa Robinson wrote (on Thu Dec 29):

do this ..

in euterpe

ln -s /n/nosferatu/s2/euterpe/verify

I currently have:

```
tbr@gamorra ~/euterpe/verilog/bsrc 605 % ls -ls ../../verify
   1 lrwxrwxrwx  1 tbr        27 Dec 11 19:10 ../../verify -> /n/rhodan/s3/euterpe/verify

tbr@gamorra ~/euterpe/verilog/bsrc 606 % ls -ls /n/rhodan/s3/euterpe/verify
   1 lrwxrwxrwx  1 lisar      30 Aug 19 12:26 /n/rhodan/s3/euterpe/verify -> /n/nosferatu/s1/euterpe/verify
```

then:
```
tbr@gamorra ~/euterpe/verilog/bsrc 607 % ls -ls /n/nosferatu/s1/euterpe/verify
   1 lrwxrwxrwx  1 lisar      22 Oct  2 12:20 /n/nosferatu/s1/euterpe/verify -> /n/nosferatu/s1/verify
```

but:
```
tbr@gamorra ~/euterpe/verilog/bsrc 609 % ls -ls /n/nosferatu/s2/euterpe/verify
   1 lrwxrwxrwx  1 lisar      22 Oct  1 12:49 /n/nosferatu/s2/euterpe/verify -> /n/nosferatu/s1/verify
```

so:

I don't think it will make any difference! All the files it's
complaining about it wants to see in bsrc, so it looks like I need to
run something to copy them from the verify area.

Tim

From:	tbr
Sent:	Friday, December 30, 1994 12:28 AM
To:	'tom'
Cc:	'doi'; 'geert'
Subject:	BOM trouble
Follow Up Flag: Follow up
Flag Status:	Red

When I did agetbom in the proteus snapshot I got the following
warning:

WARNING SUMMARY ------------------------------
/n/auspex/s23/euterpe-proteus-cp/ged/sc: Directory scxbcgdr1 is not part of the BOM (but still present locally)

I do not see this directory in /u/chip so I assume it's obsolete.
If so do you know why getbom would not have removed it? Anyway if it
is obsolete, can you clean it up manually please?

Tim

From: tbr (Tim B. Robinson)
Sent: Friday, December 30, 1994 12:28 AM
To: 'tom'
Cc: 'doi'; 'geert'
Subject: BOM trouble

When I did agetbom in the proteus snapshot I got the following
warning:

WARNING SUMMARY ------------------------------
/n/auspex/s23/euterpe-proteus-cp/ged/sc: Directory scxbcgdrl is not part of the BOM (but
still present locally)

I do not see this directory in /u/chip so I assume it's obsolete.
If so do you know why getbom would not have removed it? Anyway if it is obsolete, can you
clean it up manually please?

Tim

From: hopper (Mark Hofmann)
Sent: Friday, December 30, 1994 6:05 AM
To: 'hardheads'
Subject: 12 noon release (Virtual 10am disturbance)

Hi,

   A /u/chip re-make failed last night due to a latent bug introduced into the PIM/PIF
utilities on 16 December. The .flipx and .flipy directives had their actions interchanged.
This release should fix the bug. With the
16 December release many of Euterpe's Gards placements use the .flip?
directives in passes subsequent to pass1 (these directives are now introduced
automatically). Please let me know if you experience any turbulence.

   -thanks,
   hopper

From: tbr

Sent: Friday, December 30, 1994 10:59 AM

To: 'wampler'; 'tom'; 'hopper'

Cc: 'geert'

Subject: snapshot build

Follow Up Flag: Follow up

Flag Status: Red

Last night I fired up a make in the proteus snapshot. It seems to
have hung. It was on godzilla, and the last thing in the log file is:

/n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: 22 rows (22 non-empty)
...spanning 16 columns (16 maximum cells/row)
...for a total of 173 cells were written to `pl_mne_logic.pim.pif.0'.
/n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: (34, 2) to (162, 68) [64 by 22 ECL atoms]
/n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: 1114 ECL atoms placed in 1408 [-0 obstructions] atom area
[79.12% dense]
#pim2pif.ex Version 0.2.36 Fri Dec 16 16:45:30 PST 1994
/n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif: Concatenated output written to pl_mne_logic.pim.pif

Requires a minimum license of xgplace1_3 or gards1_3 .
Applicable licenses available at your installation :
                 gardsconfig_3
Checked out one user token of a gardsconfig_3 license.

gardslic tells me:

Users of gardsconfig_3: (Total of 10 licenses available)

chip godzilla /dev/tty (v7.115) (rhea/7576 538), start Fri 12/30 3:08

Yet according to top there is nothing going on there that I can see.

Can one of you investigate please? (BTW, it was running as chip.)

Tim

Last night I fired up a make in the proteus snapshot. It seems to have hung. It was on godzilla, and the last thing in the log file is:

    /n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: 22 rows (22
non-empty)
    ...spanning 16 columns (16 maximum cells/row)
    ...for a total of 173 cells were written to `pl_mne_logic.pim.pif.0'.
    /n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: (34, 2) to (162,
68) [64 by 22 ECL atoms]
    /n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: 1114 ECL atoms placed in 1408
[-0 obstructions] atom area [79.12% dense]
    #pim2pif.ex Version 0.2.36 Fri Dec 16 16:45:30 PST 1994
    /n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif: Concatenated output written to
pl_mne_logic.pim.pif

    Requires a minimum license of xgplace1_3 or gards1_3 .
    Applicable licenses available at your installation :
                    gardsconfig_3
    Checked out one user token of a gardsconfig_3 license.

gardslic tells me:

    Users of gardsconfig_3: (Total of 10 licenses available)

  chip godzilla /dev/tty (v7.115) (rhea/7576 538), start Fri 12/30 3:08

Yet according to top there is nothing going on there that I can see.

Can one of you investigate please? (BTW, it was running as chip.)

Tim

From:	tom (Tom Laidig)
Sent:	Friday, December 30, 1994 11:00 AM
To:	'Tim B. Robinson'
Cc:	'doi (Derek Iverson)'; 'geert (Geert Rosseel)'; 'tom (Thomas Laidig)'
Subject:	Re: BOM trouble

Tim B. Robinson writes:

> When I did agetbom in the proteus snapshot I got the following
> warning:
>
> WARNING SUMMARY ------------------------------
> /n/auspex/s23/euterpe-proteus-cp/ged/sc: Directory scxbcgdr1 is not
> part
of the BOM (but still present locally)
>
> I do not see this directory in /u/chip so I assume it's obsolete.
> If so do you know why getbom would not have removed it? Anyway if it
> is obsolete, can you clean it up manually please?

I'll let doi comment on getbom's behavior (FYI, doi, that directory only contained 4
files, all under cvs control). I have removed scxbcgdr1, since it is, in fact, obsolete.
It was deleted in BOM revision 45.0 dated 12/21:

```
    ----------------------------
    revision 45.0
    date: 1994/12/21 09:18:08 LT;  author: tom;  state: Exp;  lines: +1 -1
    Release Target: proteus/ged/sc

    delete unused scxbcgdr1 schematic
    ----------------------------
```

```
    --
    ooooO    Ooooo
    (   _)    (_   )
     \ (  tau  ) /
      (_)      (_)
```

From:	tbr

From: tbr
Sent: Friday, December 30, 1994 11:02 AM
To: 'solo (John Campbell)'
Cc: 'Tom Laidig'
Subject: Re: proteus snapshot (fwd)
Follow Up Flag: Follow up
Flag Status: Red

John Campbell wrote (on Fri Dec 30):

as Tom Laidig was saying ....

..
..FYI -- it appears the snapshot will do some major churning...

..
..Tim B. Robinson writes:
..|From tbr Thu Dec 29 21:29:55 1994
..|Date: Thu, 29 Dec 1994 21:29:50 -0800
..|From: tbr (Tim B. Robinson)
..|Message-Id: <199412300529.VAA18068@aphrodite.microunity.com>
..|To: geert
..|cc: hopper, tom, lisar
..|Subject: proteus snapshot
..|
..|
..|Since it was out of date in a number of significant respects
..|I have started up a getbom and rebuild while things are quiet.
..|

..|Tim
..|
..
..
..--
..   ooooO Ooooo
.. (_) (_)
.. \(tau)/
..   ( ) ( )
..

thanks for the info

I just mailed tom (among others). It appears to have hung:

To: wampler,tom,hopper
cc: geert
Subject: snapshot build

Last night I fired up a make in the proteus snapshot. It seems to
have hung. It was on godzilla, and the last thing in the log file is:

/n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: 22 rows (22 non-empty)
...spanning 16 columns (16 maximum cells/row)

...for a total of 173 cells were written to `pl_mne_logic.pim.pif.0'.
/n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: (34, 2) to (162, 68) [64 by 22 ECL atoms]
/n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: 1114 ECL atoms placed in 1408 [-0 obstructions] atom area
[79.12% dense]
#pim2pif.ex Version 0.2.36 Fri Dec 16 16:45:30 PST 1994
/n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif: Concatenated output written to pl_mne_logic.pim.pif

Requires a minimum license of xgplace1_3 or gards1_3 .
Applicable licenses available at your installation :
                        gardsconfig_3
Checked out one user token of a gardsconfig_3 license.

gardslic tells me:

Users of gardsconfig_3: (Total of 10 licenses available)

chip godzilla /dev/tty (v7.115) (rhea/7576 538), start Fri 12/30 3:08

Yet according to top there is nothing going on there that I can see.

Can one of you investigate please? (BTW, it was running as chip.)

Tim

From:	tom (Tom Laidig)
Sent:	Friday, December 30, 1994 11:15 AM
To:	'Tim B. Robinson'
Cc:	'wampler (Kurt Wampler)'; 'hopper (Mark Hofmann)'; 'geert (Geert Rosseel)'; 'tom (Thomas Laidig)'
Subject:	Re: snapshot build

Tim B. Robinson writes:

Last night I fired up a make in the proteus snapshot. It seems to have
hung. It was on godzilla, and the last thing in the log file is:

    /n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: 22 rows (22
non-empty)
    ...spanning 16 columns (16 maximum cells/row)
    ...for a total of 173 cells were written to `pl_mne_logic.pim.pif.0'.
    /n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: (34, 2) to
(162, 68) [64 by 22 ECL atoms]
    /n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif.ex: 1114 ECL
atoms
placed in 1408 [-0 obstructions] atom area [79.12% dense]
    #pim2pif.ex Version 0.2.36 Fri Dec 16 16:45:30 PST 1994
    /n/auspex/s23/euterpe-proteus-cp/tools/bin/pim2pif: Concatenated
output written to pl_mne_logic.pim.pif

    Requires a minimum license of xgplace1_3 or gardsl_3 .
    Applicable licenses available at your installation :
                    gardsconfig_3
    Checked out one user token of a gardsconfig_3 license.

gardslic tells me:

    Users of gardsconfig_3:   (Total of 10 licenses available)

   chip godzilla /dev/tty (v7.115) (rhea/7576 538), start Fri 12/30 3:08

Yet according to top there is nothing going on there that I can see.

Can one of you investigate please? (BTW, it was running as chip.)

It seems to be hung in gplace. The `gplace.nic' file ends with the command `exitsave'
which only exits if the placement is complete. Looking in the gplace.lis file, I find

*********************** Design status *********************************
*
*
Cpu (hrs/mins/secs)   total: 0/0/1   delta: 0/0/1
Status   dff: unplaced, unrouted   current: 169 of 173 placed
Net lengths and est routing lengths:
  Length wgted/unwgt: 25217/25217 max net wgted/unwgt: 522/522 Congestion measures and
counts:
  Cong: 0 max hor: 0/78 max ver: 0/40 max 2d: 31
Merit: 25217
*
*
***************** End design status *********************************

So for some reason, it couldn't place everything.

I'll let Kurt investigate from here (I suspect he already is, since this part of the
gplace.lis file is new), but I'll just mention that we probably want to add an

`exitnosave' command after the `exitsave'
command in the gardswart gplace.nic file(s), so gplace won't hang if it can't complete the
placement. We already use this trick in the leafmold and verilog/bsrc stuff.

--
```
    ooooO    Ooooo
    (  _)    (_  )
     \(  tau  )/
     (_)      (_)
```

Jay Some failures.

Lisa R.

Simulator: c_euterpe_wrap.mif.mm was built on Thu Dec 29 22:31:56 1994

Using BOM: Version BOM,v 198.0 1994/12/28 14:09:40 LT woody
Warning: Local BOM is out of date ...
Latest BOM is: RCS Version: 198.3 /p/cvsroot/euterpe/verilog/bsrc/BOM,v
Log Message:
Run started on host: aphrodite at: Thu Dec 29 22:38:39 PST 1994


```
              test10_0    Processing test10_0 .... Ran ok
Run time = 1267 seconds Performance = 11 cycles/second
              eshort_0    Processing eshort_0 .... Ran ok
Run time = 1528 seconds Performance = 10 cycles/second
              branch_0    Processing branch_0 .... Ran ok
Run time = 1206 seconds Performance = 11 cycles/second
              register_0    Processing register_0 .... Ran ok
Run time = 1520 seconds Performance = 10 cycles/second
               rf_0    Processing rf_0 .... Ran ok
Run time = 1245 seconds Performance = 11 cycles/second
              load_0    Processing load_0 .... Ran ok
Run time = 1321 seconds Performance = 10 cycles/second
               store_0    Processing store_0 .... Ran ok
Run time = 1371 seconds Performance = 10 cycles/second
          store_unique_0    Processing store_unique_0 .... (in fail loop) Failed
Run time = 1368 seconds Performance = 10 cycles/second
          cystoreload_0    Processing cystoreload_0 .... Ran ok
Run time = 1657 seconds Performance = 14 cycles/second
           memtest_0    Processing memtest_0 .... (looks like X's) Failed
Run time = 580.8 seconds Performance = 28 cycles/second
               ltlb_0    Processing ltlb_0 .... Ran ok
Run time = 786.2 seconds Performance = 19 cycles/second
              gtlb_0    Processing gtlb_0 .... Ran ok
Run time = 789.2 seconds Performance = 19 cycles/second
          gtlbaccess1_0    Processing gtlbaccess1_0 .... Ran ok
Run time = 3077 seconds Performance = 16 cycles/second
          gtlbaccess2_0    Processing gtlbaccess2_0 .... (looks like X's) Failed
Run time = 586 seconds Performance = 45 cycles/second
          gtlbaccess3_0    Processing gtlbaccess3_0 .... (looks like X's) Failed
Run time = 588.2 seconds Performance = 49 cycles/second
           dcacheeasy_0    Processing dcacheeasy_0 .... Ran ok
Run time = 1.421e+04 seconds Performance = 15 cycles/second
        ibuf_storeeasy_0    Processing ibuf_storeeasy_0 .... Ran ok
Run time = 811 seconds Performance = 18 cycles/second
        itag_storeeasy_0    Processing itag_storeeasy_0 .... Ran ok
```

Geert,

Questions,
1. The sapshot is where? Path please.
2. Is it practical to view individual nets (filtering by name
) and individual components on the full chip route? (on nb it seems practical but not
instantaneous.)

billz

Bill Zuravleff wrote (on Fri Dec 30):

    Geert,

    Questions,
    1. The sapshot is where? Path please.

/n/auspex/s41

    2. Is it practical to view individual nets (filtering by name
) and individual components on the full chip route? (on nb
    it seems practical but not instantaneous.)

Patience! It should be entirely practical. We did a lot of that on Calliope.

Tim

From: Dominador Tacmo [dtacmo@gaea.microunity.com]
Sent: Friday, December 30, 1994 12:21 PM
To: 'vanthof@gaea.microunity.com'
Cc: 'ong@gaea.microunity.com'; 'geert@MicroUnity.com'
Subject: ledsegdrv

Hi Dave,

I need for you to unlock ledsegdrv, found in euterpe, so I can do edits on it. Thanks.

From:	vanthof (vant)
Sent:	Friday, December 30, 1994 12:25 PM
To:	'Dominador Tacmo'
Cc:	'ong (Warren R. Ong)'; 'geert (Geert Rosseel)'; 'vanthof (Dave Van't Hof)'
Subject:	Re: ledsegdrv

```
Dominador Tacmo writes:
>
>
>Hi Dave,
>
>I need for you to unlock ledsegdrv, found in euterpe, so I can do edits
>on it. Thanks.
>

Okay, it's done.  Please let me know when it's done, so I can lock it again.

Thanks,
Dave

--
Dave Van't Hof    vanthof@microunity.com    MicroUnity Systems Engineering,
Inc.
255 Caspian Way, Sunnyvale, CA (408) 734-8100 X276   #include <std_disclaim.h> Don't blame
me, I didn't vote for him!
```

From:	billz (Bill Zuravleff)
Sent:	Friday, December 30, 1994 12:32 PM
To:	'tbr'
Cc:	'geert'; 'hopper'
Subject:	Re: Euterpe timing analysis

1. The sapshot is where? Path please.

/n/auspex/s41

Thanks. Um,.. I'm sorry, I don't see the .stat file containing said timing or a .dff file
containing the completed placement.
Could you point these out?

Thanks,
billz

Bill Zuravleff wrote (on Fri Dec 30):

    1. The sapshot is where? Path please.

  /n/auspex/s41

  Thanks. Um,.. I'm sorry, I don't see the .stat file containing
  said timing or a .dff file containing the completed placement.
  Could you point these out?

Try:

```
tbr@aphrodite /n/auspex/s41/euterpe-snapshot/euterpe/verilog/bsrc/gards
513 % ls *.stat
chip_euterpe-final.stat chip_euterpe-iter.stat   chip_euterpe-pass1.stat tbr@aphrodite
/n/auspex/s41/euterpe-snapshot/euterpe/verilog/bsrc/gards
514 % ls *.dff
chip_euterpe-iter.dff
```

From:	tbr
Sent:	Friday, December 30, 1994 2:39 PM
To:	'woody'
Subject:	dpelgcshort_0
Follow Up Flag:	Follow up
Flag Status:	Red

There is a dump file in my ~/euterpe/verilog/bsrc. Lisar thinks this may be related to the problem with memtest.

Tim

From:	tbr
Sent:	Friday, December 30, 1994 4:02 PM
To:	'woody (Jay Tomlinson)'
Cc:	'lisar'
Subject:	dpelgcshort_0
Follow Up Flag:	Follow up
Flag Status:	Red

Jay Tomlinson wrote (on Fri Dec 30):

Tim B. Robinson wrote (on Fri Dec 30):

There is a dump file in my ~/euterpe/verilog/bsrc. Lisar thinks this
may be related to the problem with memtest.

Tim
This is probably the problem with a lot of tests, SRevntUnMskdS20 is always X.
As far as I can tell it isn't the channels that are causing the problem.

gtlbaccess2 (out of ibuf) also has this problem. I am doing a local run now
with SR dumped to isolate the problem. I will continue to look around and keep
you posted.

Thanks. I hope there is a common cause to many of the failures.
It's a little depressing right now!

Tim

From:	solo (John Campbell)
Sent:	Saturday, December 31, 1994 10:28 AM
To:	'John Campbell'
Cc:	'tom (Thomas Laidig)'; 'lisar (Lisa Robinson)'; 'vo (Tom Vo)'; 'hopper (Mark Hofmann)'; 'geert (Geert Rosseel)'; 'vanthof (Dave Van't Hof)'
Subject:	Re: VerifyRun test

Report included because i was testing yesterday and forgot to reinstantiate the
distribution list. as you recall i ran all /u/chip custom blocks. as you can see, the
run was clean.

in fact cache drc and lvs are still in queue. i am going to delay
tomorows(GMT) run till about 8am(PST) to allow cache to finish before it goes again.
should easily finish.

i guess it is known who is dinking with cli etc and what is being done.
does anyone in this group know? i like knowing these things so i don't worry about what
is happening.

as John Campbell was saying ....
..
..
..
..The following differences were noticed since Yesterday.
..in /n/auspex/s24/solo/test/compass/vlsi.boo and check.list
..---
..
..-----------------------
..CELLNAME cache
..-----------------------
..CELLNAME cli
..5c5
..< cli.ly   Mismatch RCS = 13.10 release = 13.8
..---
..> cli.ly   Mismatch RCS = 13.9 release = 13.8
..-----------------------
..CELLNAME ealnf20s6x3a
..3c3
..< /u/chip/euterpe/proteus/compass/layouts/ealnf20s6x3a.ly   13.6
Dec 30 16:56:51 1994
..---
..> /u/chip/euterpe/proteus/compass/layouts/ealnf20s6x3a.ly   13.5
Oct 31 14:11:04 1994
..-----------------------
..CELLNAME ledsegdrv
..5d4
..< ledsegdrv.ly   Mismatch RCS = 13.4 release = 13.3
..
....
..The following mismatches were found between the released Version ..cell or sub cells and
the Version found in RCS.
..You may want to release the later version, maybe not.
..
..cli.ly   Mismatch RCS = 13.10 release = 13.8
..ledsegdrv.ly   Mismatch RCS = 13.4 release = 13.3
..
....
..The following layouts were run today. This means either a change in ..the schematic or
layout.
..
..Lvslog:12/31/94 01:26 GMT running lvs -drac L cr vs S cr -large
..Lvslog:12/31/94 01:28 GMT running lvs -drac L gtlb vs   S gtlb -large

..Lvslog:12/31/94 01:48 GMT running lvs -drac L cache vs   S cache -large

```
..Lvslog:12/31/94 01:48 GMT running lvs -drac L bellybutt vs   S bellybutt

..Lvslog:12/31/94 01:49 GMT running lvs -drac L bg3stack vs   S bg3stack

..Lvslog:12/31/94 01:49 GMT running lvs -drac L bgbbcstm vs   S bgbbcstm

..Lvslog:12/31/94 01:49 GMT running lvs -drac L bgeckbb vs   S bgeckbb

..Lvslog:12/31/94 01:50 GMT running lvs -drac L bgiref vs   S bgiref
..Lvslog:12/31/94 01:56 GMT running lvs -drac L bgknobgen vs   S bgknobgen

..Lvslog:12/31/94 01:58 GMT running lvs -drac L bgproca2d vs   S bgproca2d

..Lvslog:12/31/94 02:01 GMT running lvs -drac L bgvrslv2 vs   S bgvrslv2

..Lvslog:12/31/94 02:05 GMT running lvs -drac L cedmctrl_b vs   S
/n/ghidra/s4/vo/euterpe/verilog/bsrc/ce/cedmctrlt.sp
..Lvslog:12/31/94 02:09 GMT running lvs -drac L cedmctrl_c vs   S
/n/ghidra/s4/vo/euterpe/verilog/bsrc/ce/cedmctrlt.sp
..Lvslog:12/31/94 02:18 GMT running lvs -drac L cedmctrl_m vs   S
/n/ghidra/s4/vo/euterpe/verilog/bsrc/ce/cedmctrlm.sp
..Lvslog:12/31/94 02:20 GMT running lvs -drac L cedmctrl_t vs   S
/n/ghidra/s4/vo/euterpe/verilog/bsrc/ce/cedmctrlt.sp
..Lvslog:12/31/94 02:24 GMT running lvs -drac L ceinvx5 vs   S ceinvx5

..Lvslog:12/31/94 02:28 GMT running lvs -drac L ceprobe vs   S ceprobe

..Lvslog:12/31/94 02:30 GMT running lvs -drac L cerpokgen vs   S cerpokgen

..Lvslog:12/31/94 02:36 GMT running lvs -drac L cgeb vs   S cgeb
..Lvslog:12/31/94 02:37 GMT running lvs -drac L cgeb2 vs   S cgeb2
..Lvslog:12/31/94 02:43 GMT running lvs -drac L cgeb2mast vs   S cgeb2

..Lvslog:12/31/94 02:43 GMT running lvs -drac L cgebmast vs   S cgeb
..Lvslog:12/31/94 02:49 GMT running lvs -drac L cgebns vs   S cgeb
..Lvslog:12/31/94 02:50 GMT running lvs -drac L cged vs   S cged
..Lvslog:12/31/94 02:55 GMT running lvs -drac L cli vs   S cli
..Lvslog:12/31/94 02:57 GMT running lvs -drac L ctag vs   S ctag
..Lvslog:12/31/94 03:01 GMT running lvs -drac L ea1plqh3s4x2a vs   S
ea1plqh3s4x2a -V
..Lvslog:12/31/94 03:05 GMT running lvs -drac L ea1porl4nf8s3x3a vs   S
ea1porl4nf8s3x3a -V
..Lvslog:12/31/94 03:07 GMT running lvs -drac L ea1porl5nf8s3x4a vs   S
ea1porl5nf8s3x4a -V
..Lvslog:12/31/94 03:13 GMT running lvs -drac L ea1porl6nf8s3x4a vs   S
ea1porl6nf8s3x4a -V
..Lvslog:12/31/94 03:21 GMT running lvs -drac L ea1porl7nf8s3x4a vs   S
ea1porl7nf8s3x4a -V
..Lvslog:12/31/94 03:28 GMT running lvs -drac L eaffdh16s11x2a vs   S
eaffdh16s11x2a -V
..Lvslog:12/31/94 03:35 GMT running lvs -drac L eaffbbdh12s11x2a vs   S
eaffbbdh12s11x2a -V
..Lvslog:12/31/94 03:43 GMT running lvs -drac L eaffbdh16s11x2a vs   S
eaffbdh16s11x2a -V
..Lvslog:12/31/94 03:50 GMT running lvs -drac L ealdf12s3x4a vs   S
ealdf12s3x4a -V
..Lvslog:12/31/94 03:58 GMT running lvs -drac L ealdf24s6x4a vs   S
ealdf24s6x4a -V
..Lvslog:12/31/94 04:04 GMT running lvs -drac L ealnf20s6x3a vs   S
ealnf20s6x3a -V
..Lvslog:12/31/94 04:11 GMT running lvs -drac L ealnf36s12x3a vs   S
ealnf36s12x3a -V
..Lvslog:12/31/94 04:19 GMT running lvs -drac L ealnf36s9x4a vs   S
ealnf36s9x4a -V
..Lvslog:12/31/94 04:25 GMT running lvs -drac L eam2ffdh16s11x2a vs   S
eam2ffdh16s11x2a -V
..Lvslog:12/31/94 04:33 GMT running lvs -drac L eamema1r1wi6x1a vs   S
```

```
eamemalrlwi6xla
..Lvslog:12/31/94 04:41 GMT running lvs -drac L eamemalrlwip6xla vs    S
eamemalrlwip6xla
..Lvslog:12/31/94 04:49 GMT running lvs -drac L eamemalrlwipr6xla vs    S
eamemalrlwipr6xla
..Lvslog:12/31/94 04:56 GMT running lvs -drac L eamemalrlwir6xla vs    S
eamemalrlwir6xla
..Lvslog:12/31/94 05:04 GMT running lvs -drac L eamemalrlwp6xla vs    S
eamemalrlwp6xla
..Lvslog:12/31/94 05:05 GMT running lvs -drac L eamemalrlwpr6xla vs    S
eamemalrlwpr6xla
..Lvslog:12/31/94 05:10 GMT running lvs -drac L eamemalrlwr6xla vs    S
eamemalrlwr6xla
..Lvslog:12/31/94 05:11 GMT running lvs -drac L eawwlvref16s2x4a vs    S
eawwlvref16s2x4a -V
..Lvslog:12/31/94 05:16 GMT running lvs -drac L eawwlvref20s10xla vs    S
eawwlvref20s10xla
..Lvslog:12/31/94 05:19 GMT running lvs -drac L eawwlvref56s7x4a vs    S
eawwlvref56s7x4a -V
..Lvslog:12/31/94 05:22 GMT running lvs -drac L iobufdh4s vs    S iobufdh4s

..Lvslog:12/31/94 05:27 GMT running lvs -drac L leddigdrv vs    S leddigdrv

..Lvslog:12/31/94 05:28 GMT running lvs -drac L ledkbdip vs    S ledkbdip

..Lvslog:12/31/94 05:34 GMT running lvs -drac L ledsegdrv vs    S ledsegdrv

..Lvslog:12/31/94 05:37 GMT running lvs -drac L pl_euh vs    S pl_euh
..Lvslog:12/31/94 05:40 GMT running lvs -drac L pl_eus vs    S pl_eus
..Lvslog:12/31/94 05:44 GMT running lvs -drac L sccgbfr0 vs    S sccgbfr0

..Lvslog:12/31/94 05:45 GMT running lvs -drac L sccgdr vs    S sccgdr
..Lvslog:12/31/94 05:51 GMT running lvs -drac L scioff vs    S scioff
..Lvslog:12/31/94 06:04 GMT running lvs -drac L scsynchll vs    S scsynchll

..Lvslog:12/31/94 06:10 GMT running lvs -drac L serbiflop vs    S serbiflop

..Lvslog:12/31/94 06:12 GMT running lvs -drac L sertriflop vs    S
sertriflop
..Lvslog:12/31/94 06:16 GMT running lvs -drac L tsensa vs    S tsensa
..Lvslog:12/31/94 06:20 GMT running lvs -drac L ttl3vnew vs    S ttl3vnew

..Lvslog:12/31/94 06:22 GMT running lvs -drac L ttle2ttl vs    S ttle2ttl

..Lvslog:12/31/94 06:28 GMT running lvs -drac L xcdecsw vs    S xcdecsw

..Lvslog:12/31/94 06:28 GMT running lvs -drac L xcecl2cmos vs    S
xcecl2cmos
..Lvslog:12/31/94 06:36 GMT running lvs -drac L xcinvc vs    S xcinvc
..Lvslog:12/31/94 06:37 GMT running lvs -drac L xcinvc4 vs    S xcinvc4

..Lvslog:12/31/94 06:42 GMT running lvs -drac L xclatbc vs    S xclatbc

..Lvslog:12/31/94 06:44 GMT running lvs -drac L xcmux2 vs    S xcmux2
..Lvslog:12/31/94 06:48 GMT running lvs -drac L xcmux3 vs    S xcmux3
..Lvslog:12/31/94 06:51 GMT running lvs -drac L xcnand2c vs    S xcnand2c

..Lvslog:12/31/94 06:54 GMT running lvs -drac L xcnand3c vs    S xcnand3c

..Lvslog:12/31/94 06:58 GMT running lvs -drac L xcnand4c vs    S xcnand4c

..Lvslog:12/31/94 07:01 GMT running lvs -drac L xcnrlatbc vs    S xcnrlatbc

..Lvslog:12/31/94 07:06 GMT running lvs -drac L xcvffsw vs    S xcvffsw

..Lvslog:12/31/94 07:07 GMT running lvs -drac L xcvrrsw vs    S xcvrrsw

..Lvslog:12/31/94 07:12 GMT running lvs -drac L xcweakc vs    S xcweakc
```

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..Lvslog:12/31/94 07:14 GMT running lvs -drac L sc2p8 vs    S sc2p8
..Lvslog:12/31/94 07:19 GMT running lvs -drac L scsmf3v3 vs    S scsmf3v3

..Lvslog:12/31/94 07:21 GMT running lvs -drac L scsof1 vs    S scsof1
..Lvslog:12/31/94 07:25 GMT running lvs -drac L sc1p3 vs    S sc1p3
..Lvslog:12/31/94 07:29 GMT running lvs -drac L scsmf3rv3 vs    S scsmf3rv3

..Lvslog:12/31/94 07:31 GMT running lvs -drac L scsmf2 vs    S scsmf2
..Lvslog:12/31/94 07:36 GMT running lvs -drac L sc2p3 vs    S sc2p3
..Lvslog:12/31/94 07:38 GMT running lvs -drac L sc1p8 vs    S sc1p8
..Lvslog:12/31/94 07:42 GMT running lvs -drac L scsdm8bv3 vs    S scsdm8bv3
-V
..Lvslog:12/31/94 07:46 GMT running lvs -drac L scsmf1 vs    S scsmf1
..Lvslog:12/31/94 07:48 GMT running lvs -drac L scsdm8 vs    S scsdm8 -V

..Lvslog:12/31/94 07:53 GMT running lvs -drac L scsof3v3 vs    S scsof3v3
-V
..Lvslog:12/31/94 07:54 GMT running lvs -drac L scsdm16 vs    S scsdm16 -V

..Lvslog:12/31/94 08:01 GMT running lvs -drac L scioffdf16s vs    S
scioffdf16s
..Lvslog:12/31/94 08:01 GMT running lvs -drac L scsd4x2 vs    S scsd4x2 -V

..Lvslog:12/31/94 08:07 GMT running lvs -drac L scxbbufdh12s vs    S
scxbbufdh12s
..Lvslog:12/31/94 08:09 GMT running lvs -drac L scxbcgbfr0 vs    S
scxbcgbfr0
..Lvslog:12/31/94 08:13 GMT running lvs -drac L scxbcgdr0 vs    S scxbcgdr0

..Lvslog:12/31/94 08:17 GMT running lvs -drac L scxbef02p2s vs    S
scxbef02p2s
..Lvslog:12/31/94 08:18 GMT running lvs -drac L scxbef12p2s vs    S
scxbef12p2s
..Lvslog:12/31/94 08:24 GMT running lvs -drac L scxbef2s vs    S scxbef2s

..Lvslog:12/31/94 08:25 GMT running lvs -drac L scxbmux2dh12s vs    S
scxbmux2dh12s
..Lvslog:12/31/94 08:30 GMT running lvs -drac L scxbmux2dh16s vs    S
scxbmux2dh16s
..Lvslog:12/31/94 08:33 GMT running lvs -drac L scsof2 vs    S scsof2
..Lvslog:12/31/94 08:36 GMT running lvs -drac L xbc01df4s vs    S xbc01df4s

..Lvslog:12/31/94 08:40 GMT running lvs -drac L iobyte vs    S iobyte
..Drclog:12/31/94 01:15 GMT running DRC -iss L cr    -large
..Drclog:12/31/94 01:16 GMT running DRC -iss    -large  on gtlb
..Drclog:12/31/94 01:17 GMT running DRC -iss    -large  on cache
..Drclog:12/31/94 01:20 GMT running DRC -drac    -V  on ealnf20s6x3a
..Drclog:12/31/94 01:22 GMT running DRC -drac    on sccgbfr0
..
..........................................................................
..The following cells may have bad lvs results.  Check it out.
..
.......Circuit DISCREPANCIES
..
..
..........................................................................
..Possible Other Problems
..
..Did not find output file for cache.lvs ..Did not find output file for cache.err ..
..........................................................................
..The following cells may have bad drc results.  Check it out.
..
..Possible ERROR drc.cache may be stuck in queue or just slow ..
..........................................................................
..The following cells may have shorts or opens.
..
```

....
regards,
solo a.k.a. John Campbell   x516